T4240RDB-B

» T4240
» T4160

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Revisions

Rev	Description	Date	Approved
DX1	Release A055	2023_0227	G. Milliorn
DX2	1. CS4340 (obsolete/LL) changed to 2x TI DS100DF410 2. Clock for CS4340 (MC100LVEP14DTG) deleted. 3. U599/IDR 8L30205NLGI (52W) deleted. 4. Updated U130 to prog. part (SI5341B-D15297-GM). 5. Replaced T4240 assembly with T4240 alone. 6. Replaced obs. SATA connector w/Molex 67800-5025 7. Replaced obs. AT24C02 w/24AA025UID-I/SN (2x).	2023_0321	G. Milliorn
DX3+	1. Replace SD translator. 2. Remove NAND flash and change device. 3. Add pullups to EVT* and pulldowns to SD*_RX if unused. 4. Increase 10G SD caps to 0.22uF 5. Replace SYS/DDR clock select mux. 6. Replace obsolete enet jacks with BEL	2023_0421	G. Milliorn
E	Release A085	2023_1026	G. Milliorn

NOTES:

1. All information is subject to change without notice. No warranty, expressed or applied, is made as to the accuracy of the information contained herein. This schematic is provided for reference purposes only. Contact your NXP representative to obtain the latest information on this product or related products.

2. All resistors are 0402 1/10W 5% unless otherwise noted.

3. All capacitors are 0402 X5R/X7R 10% unless otherwise noted.

4. All components are 0C to 85C unless otherwise noted.

5. PCB stackups are provided for reference only, and may be slightly modified by PCB vendor firms as needed.

6. This design is not certified to industrial or automotive temperature ranges. Components may be rated for AEC-Q200 but this is merely incidental.

7. Errata corrections are noted with "E-nnnnn" in red boxes. For full details, consult the board errata: T4240RDB-ER

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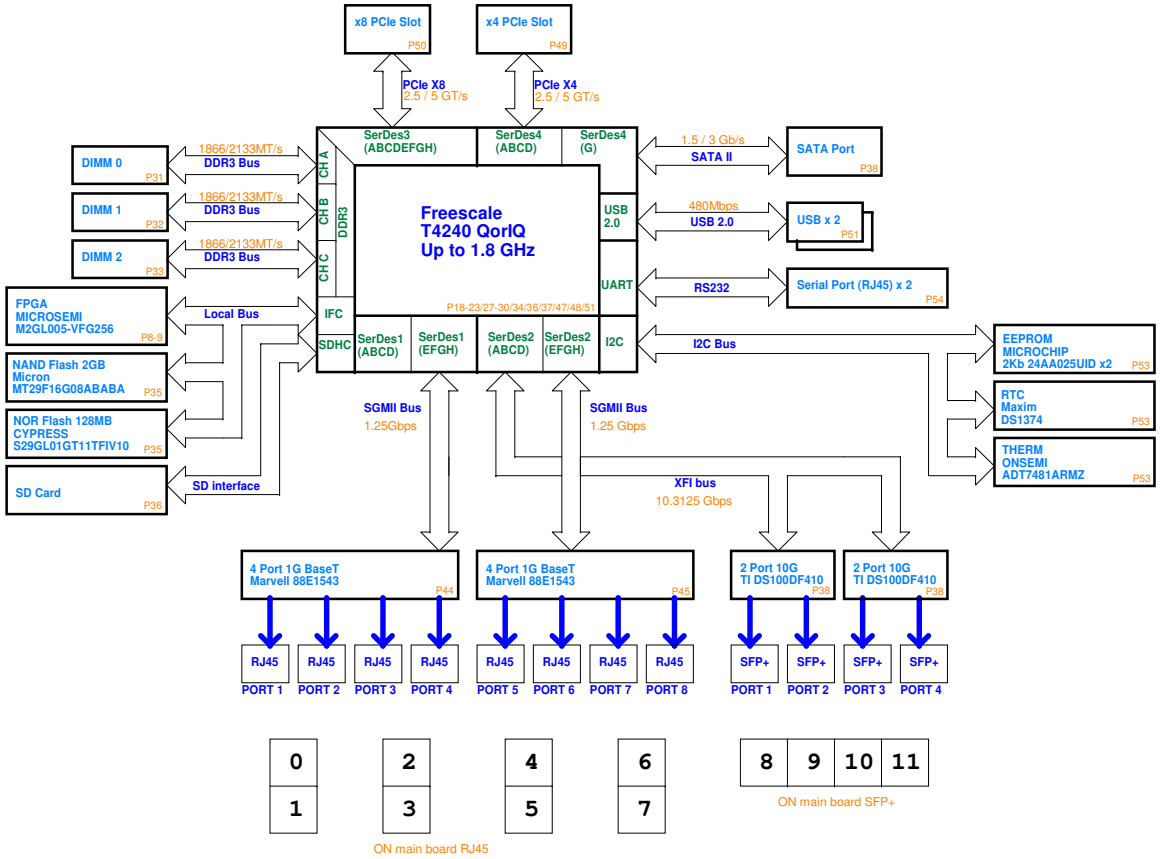
BLOCK DIAGRAM



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STACKUP

Lyr	Image	Mat.Type	Foil	CU%	Cu Type	DK[MAT]	DF[MAT]	Mat.Info	Cal.Thk	Avg.Cu Thk
TO										
TS										
TL		Foil	0.33oz	55	HTE					2.1mil
		Prepreg				3.8		EM-827B 1080 RC68%	3.06mil	
L2		Core	1oz	72	RTF	4.19	0.019	EM-827 2113*1	3.50mil	1.2mil
L3			0.5oz	38	RTF					0.6mil
		Prepreg				3.59	0.024	EM-827B 106 RC76%		
		Prepreg				3.59	0.024	EM-827B 106 RC76%	4.29mil	
L4		Core	1oz	72	RTF	4.19	0.019	EM-827 2113*1	3.50mil	1.2mil
L5			0.5oz	38	RTF					0.6mil
		Prepreg				3.59	0.024	EM-827B 106 RC76%		
		Prepreg				3.59	0.024	EM-827B 106 RC76%	4.29mil	
L6		Core	1oz	72	RTF	4.19	0.019	EM-827 2113*1	3.50mil	1.2mil
L7			0.5oz	38	RTF					0.6mil
		Prepreg				3.59	0.024	EM-827B 106 RC76%		
		Prepreg				3.59	0.024	EM-827B 106 RC76%	4.29mil	
L8		Core	1oz	72	RTF	3.98	0.021	EM-827 1086*1	2.99mil	1.2mil
L9			1oz	72	RTF					1.2mil
		Prepreg				3.59	0.024	EM-827B 106 RC76%		
		Prepreg				3.59	0.024	EM-827B 106 RC76%	4.29mil	
L10		Core	0.5oz	38	RTF	4.19	0.019	EM-827 2113*1	3.50mil	0.6mil
L11			1oz	72	RTF					1.2mil
		Prepreg				3.59	0.024	EM-827B 106 RC76%		
		Prepreg				3.59	0.024	EM-827B 106 RC76%	4.29mil	
L12		Core	0.5oz	38	RTF	4.19	0.019	EM-827 2113*1	3.50mil	0.6mil
L13			1oz	72	RTF					1.2mil
		Prepreg				3.59	0.024	EM-827B 106 RC76%		
		Prepreg				3.59	0.024	EM-827B 106 RC76%	4.29mil	
L14		Core	0.5oz	38	RTF	4.19	0.019	EM-827 2113*1	3.50mil	0.6mil
L15			1oz	72	RTF					1.2mil
		Prepreg				3.8		EM-827B 1080 RC68%	3.06mil	
BL		Foil	0.33oz	55	HTE					2.1mil
BS										
BO										

Index 次序	Index 层别	Group 组别	Ref Layer 参考层			Customer Design 客户设计						Calculated Result 计算后值				
			Up 上	Down 下	Self 当前	Imp. Mode 阻抗模型	Target Imp. 成品阻抗Ω	Tolerance 公差Ω	Line Width 线 宽	Line Space 线 距	L 2 Cu 线2铜	Line Width 线 宽	Line Space 线 距	L 2 Cu 线2铜	Calculated 计算阻抗Ω	Remark 备注
1	L01			L02		se_coated_microstrip	50.0	±5.0	5.00	—	—	4.64	—	—	50.00	
2	L01			L02		diff_coated_microstrip	85.0	±8.5	4.70	5.30	—	4.70	5.30	—	84.26	
3	L01			L02		diff_coated_microstrip	90.0	±9.0	4.00	4.00	—	3.60	4.40	—	89.10	
4	L01			L02		diff_coated_microstrip	100.0	±10.0	4.00	7.00	—	3.60	7.40	—	99.30	
5	L03		L04	L02		se_stripline	50.0	±5.0	3.50	—	—	3.43	—	—	50.01	
6	L03		L04	L02		diff_stripline	90.0	±9.0	4.00	6.00	—	3.92	6.08	—	90.00	
7	L03		L04	L02		diff_stripline	100.0	±10.0	3.50	10.00	—	3.37	10.13	—	100.00	
8	L03		L04	L02		diff_stripline	85.0	±8.5	4.00	4.00	—	4.00	4.00	—	84.65	
9	L05		L06	L04		se_stripline	50.0	±5.0	3.50	—	—	3.43	—	—	50.01	
10	L05		L06	L04		diff_stripline	90.0	±9.0	4.00	6.00	—	3.92	6.08	—	90.00	
11	L05		L06	L04		diff_stripline	100.0	±10.0	3.50	10.00	—	3.37	10.13	—	100.00	
12	L05		L06	L04		diff_stripline	85.0	±8.5	4.00	4.00	—	4.00	4.00	—	84.65	
13	L07		L08	L06		se_stripline	50.0	±5.0	3.50	—	—	3.43	—	—	50.01	
14	L07		L08	L06		diff_stripline	90.0	±9.0	4.00	6.00	—	3.92	6.08	—	90.00	
15	L07		L08	L06		diff_stripline	100.0	±10.0	3.50	10.00	—	3.37	10.13	—	100.00	
16	L07		L08	L06		diff_stripline	85.0	±8.5	4.00	4.00	—	4.00	4.00	—	84.65	
17	L10		L09	L11		se_stripline	50.0	±5.0	3.50	—	—	3.43	—	—	50.01	
18	L10		L09	L11		diff_stripline	90.0	±9.0	4.00	6.00	—	3.92	6.08	—	90.00	
19	L10		L09	L11		diff_stripline	100.0	±10.0	3.50	10.00	—	3.37	10.13	—	100.00	
20	L10		L09	L11		diff_stripline	85.0	±8.5	4.00	4.00	—	4.00	4.00	—	84.65	
21	L12		L11	L13		se_stripline	50.0	±5.0	3.50	—	—	3.43	—	—	50.01	
22	L12		L11	L13		diff_stripline	90.0	±9.0	4.00	6.00	—	3.92	6.08	—	90.00	
23	L12		L11	L13		diff_stripline	100.0	±10.0	3.50	10.00	—	3.37	10.13	—	100.00	
24	L12		L11	L13		diff_stripline	85.0	±8.5	4.00	4.00	—	4.00	4.00	—	84.65	
25	L14		L13	L15		se_stripline	50.0	±5.0	3.50	—	—	3.43	—	—	50.01	
26	L14		L13	L15		diff_stripline	90.0	±9.0	4.00	6.00	—	3.92	6.08	—	90.00	
27	L14		L13	L15		diff_stripline	100.0	±10.0	3.50	10.00	—	3.37	10.13	—	100.00	
28	L14		L13	L15		diff_stripline	85.0	±8.5	4.00	4.00	—	4.00	4.00	—	84.65	
29	L16			L15		se_coated_microstrip	50.0	±5.0	5.00	—	—	4.64	—	—	50.00	
30	L16			L15		diff_coated_microstrip	85.0	±8.5	4.70	5.30	—	4.70	5.30	—	84.26	
31	L16			L15		diff_coated_microstrip	90.0	±9.0	4.00	4.00	—	3.60	4.40	—	89.10	
32	L16			L15		diff_coated_microstrip	100.0	±10.0	4.00	7.00	—	3.60	7.40	—	99.30	

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POWER TREE

Power Supply	V	Max A	Max W	Req. A	Req. W	Eff%	12V0	5V0	3V3	5V0_SB	3V3_SB	1V8 _SB	1V2_ FPGA	1V35 XVDD	1V0 VDD	1V8 OVDD	1V5 GVDD	VTT_A	VTT_B	2V5	1V89	1V0	M VREF
							Loads (A)																
							12.0	5.0	3.3	5.0	3.3	1.8	1.2	1.35	1	1.8	0.75	0.75	0.75	2.5	1.89	1.0	0.75
ATX PSU	-	-	250	-	203	90%	6.604	17.8013	9.663	0.5136													
RT9013-33GQW	3.3	0.5	1.65	0.33	1.08	80%				0.3936	0.328												
RT9013-18GB	1.8	0.5	0.9	0.1	0.18	80%				0.12		0.1											
RT9078-12GJ5_5P	1.2	0.3	0.36	0.05	0.06	85%					0.0575		0.05										
AP62600SJ-7	1.35	6	8.1	3.95	5.34	85%	0.52306							3.952									
LTC3882	1	70	70	67	67	85%		15.7713							67.028								
AP62600SJ-7	1.8	6	10.8	2.5	4.51	85%	0.44171									2.503							
LTC7150S	1.8	20	36	2.5	4.51	85%	0.44171										13.84						
MP20073DH VTT	0.75	2	1.5	2	1.5	79%			0.003								2.42	2					
MP20073DH VTT	0.75	2	1.5	2	1.5	79%			0.003								2.42		2				
AP62600SJ-7	2.5	6	15	1.62	4.05	85%	0.39706													1.62			
MAX8902B	1.89	0.5	0.95	0.18	0.33	85%															0.176		
AP62600SJ-7	1	6	6	0.56	0.56	85%																0.56	
MP20073DH VREF *2	0.8	0.02	0.02	0.03	0.02	79%																	0.03
CURRENT LOADS GROUPED BY DEVICE BY RAIL							4.80	2.03	9.66	0.00	0.27	0.10	0.05	3.95	67.03	2.50	9.00	2.00	2.00	1.62	0.18	0.56	0.03 A

I2C DEVICE TREE

```
I2C1
+-- n/a        Header
+-- 0x4C       ADT7481 Thermal Monitor
+-- 0x4D       EMC2305 Fan Controller
+-- 0x50       I2C Boot Rom, 2Kb
+-- 0x51       PCF2131 Real-Time Clock
+-- 0x52       DDR3 #1 SPD EEPROM
+-- 0x54       DDR3 #2 SPD EEPROM
+-- 0x56       DDR3 #3 SPD EEPROM
+-- 0x57       System ID EEPROM, 256B
+-- 0x63       LTC3882 (VDD)
+-- 0x66/67    System Control FPGA BCSRs
+-- 0x74       Si5341B Clock Synthesizer
+-- 0x75       PCA9547 (I2C mux, level 2)
+-- I2C1_CH0
    +-- 0x18   DS100DF410 Retimer #1
    +-- 0x19   DS100DF410 Retimer #2
+-- I2C1_CH1
    +-- 0x50   SFP+ Cage #1 (10GE Retimer #1)
+-- I2C1_CH2
    +-- 0x50   SFP+ Cage #1 (10GE Retimer #1)
+-- I2C1_CH3
    +-- 0x50   SFP+ Cage #1 (10GE Retimer #2)
+-- I2C1_CH4
    +-- 0x50   SFP+ Cage #1 (10GE Retimer #2)
+-- I2C1_CH5
+-- I2C1_CH6
    +-- ????   PCIe Slot #1
+-- 0x50       SFP+ Cage #2 (25G PHY #2)
+-- I2C1_CH7
    +-- 0x20   SFP Monitor/Control GPIO
    +-- 0x7C   SFP Monitor/Control Reset
I2C2 - n/a
    +-- ????   PCIe Slot #2

NOTE: All I2C addresses are 7-bit (no RW bit),
      as are used with uboot
```

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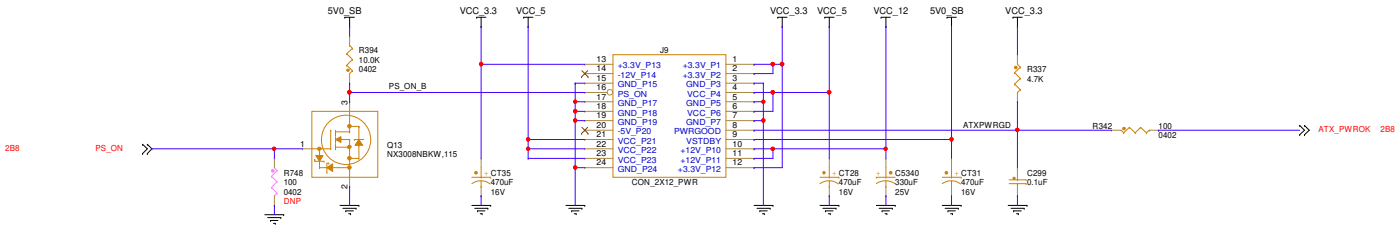
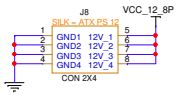
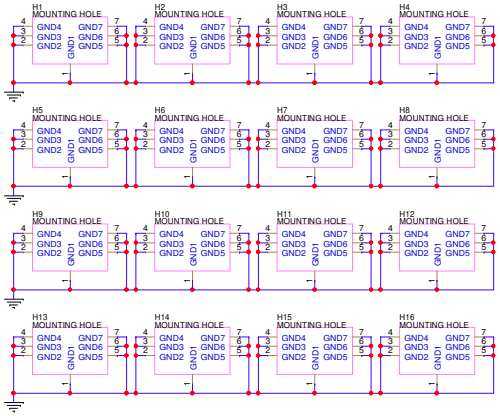
ATX POWER + MECH





VCC_12_8P
- Used only by VDD supply



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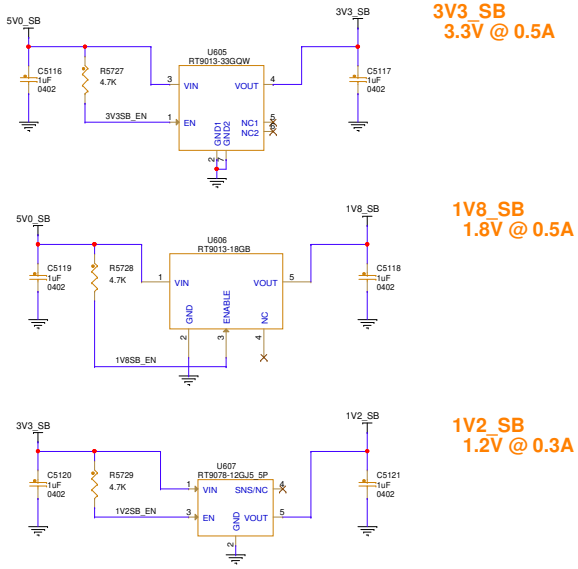
STANDBY POWER



3V3_SB
3.3V @ 0.5A

1V8_SB
1.8V @ 0.5A

1V2_SB
1.2V @ 0.3A

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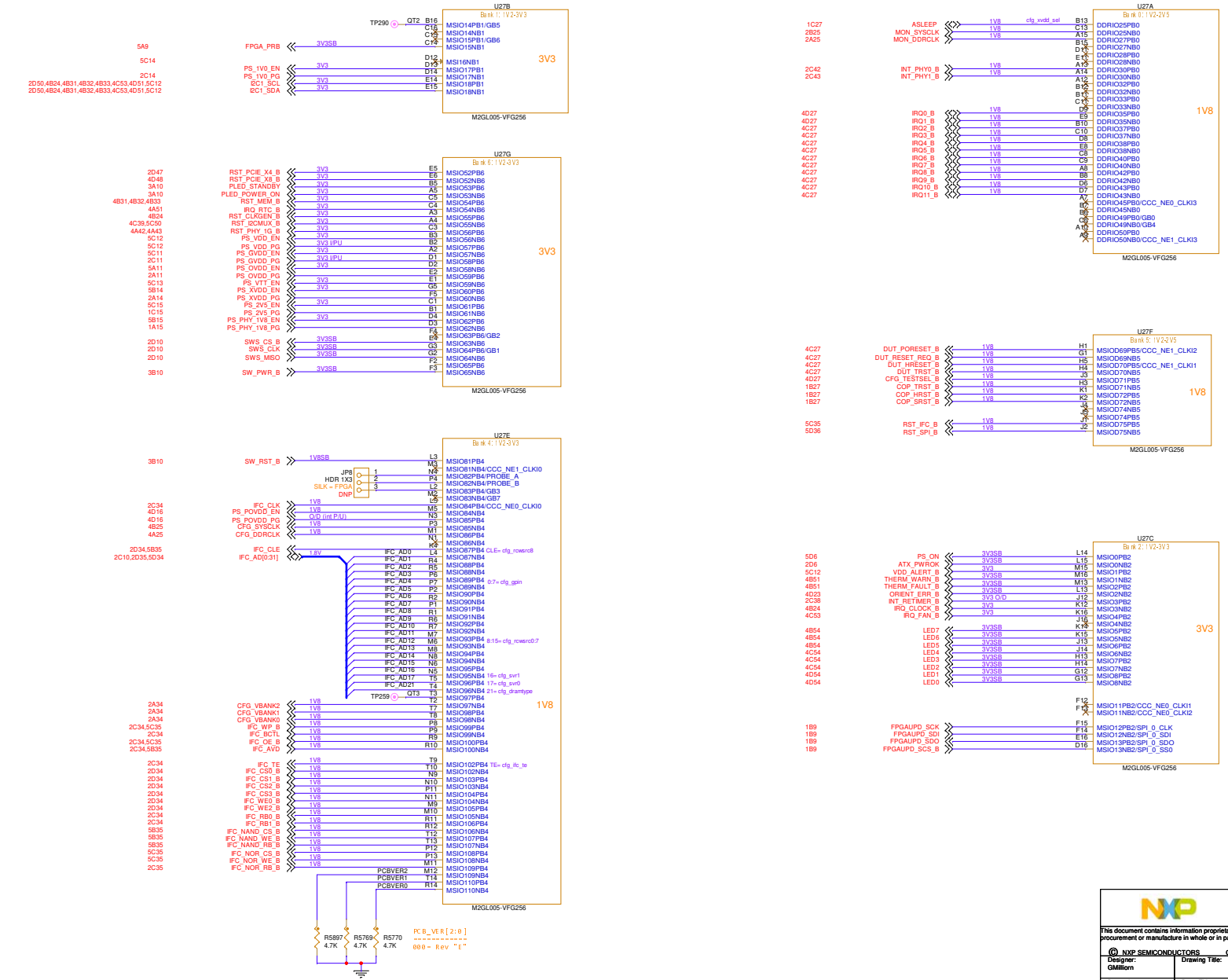
FPGA: IO PORTS



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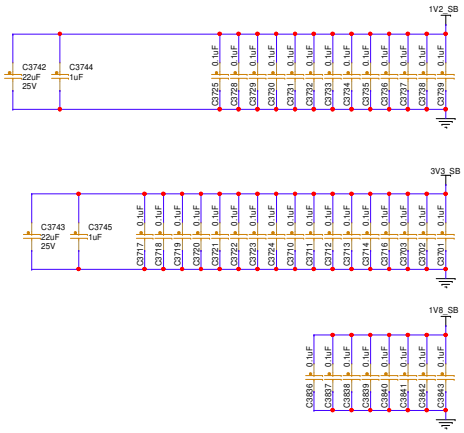
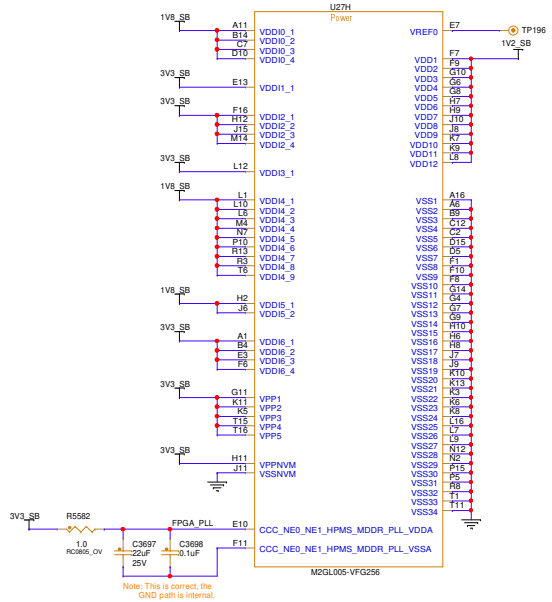
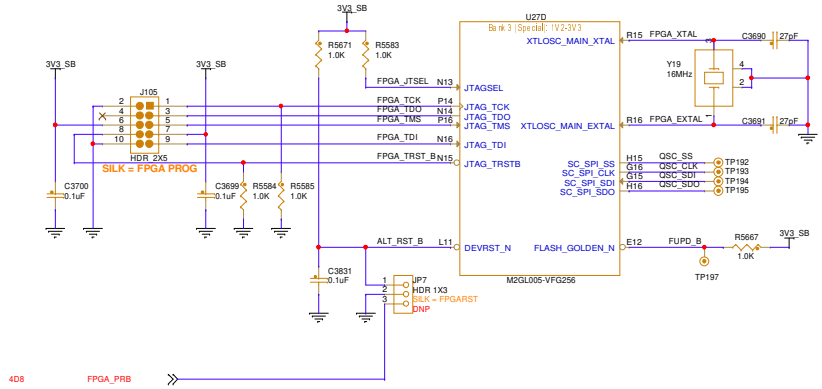
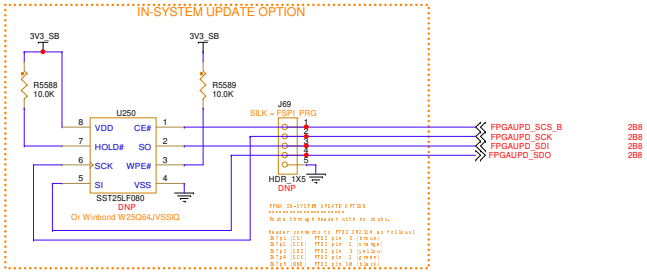
FPGA: POWER & PROGRAM









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Drawn by: GMillorn	Page Title: FPGA Power & Program		
Approved: DN_Apps	Size C	Document Number SCH-27749 / PDF: SPF-27749	Rev E
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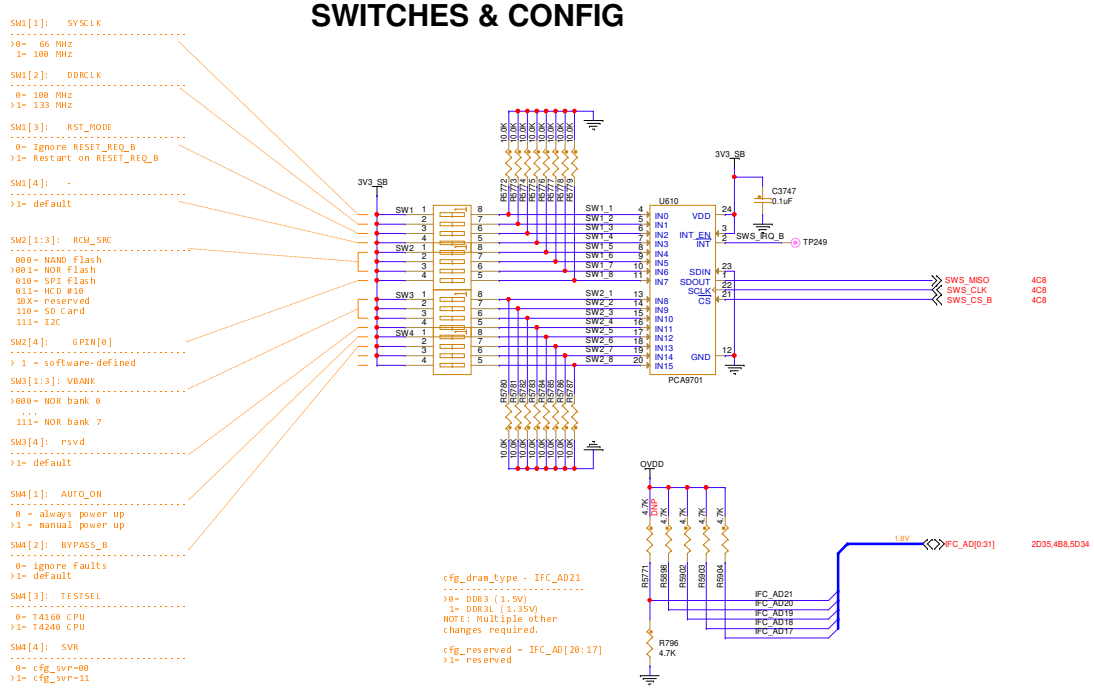
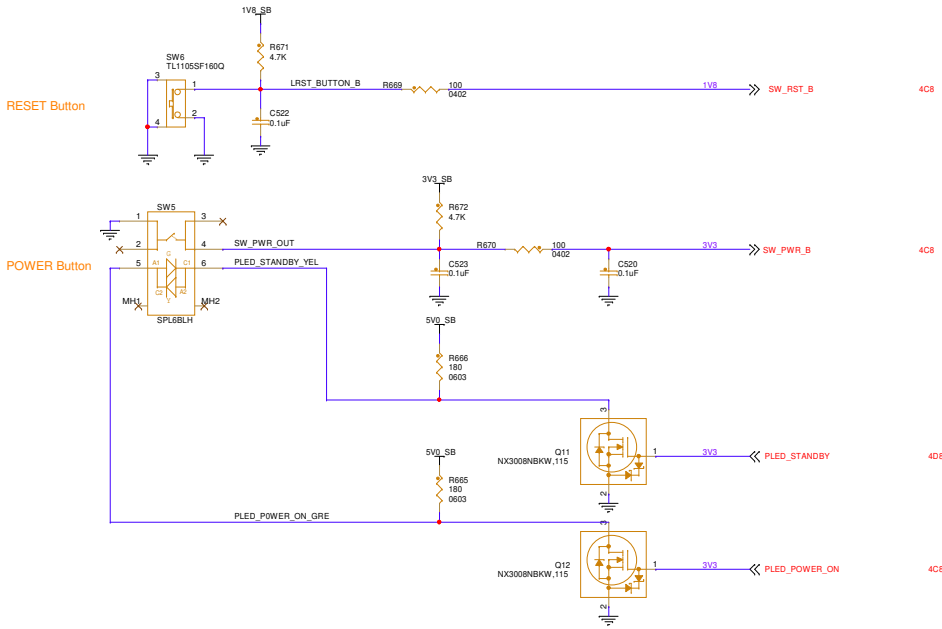
SWITCHES & CONFIG





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Approved: DN_Apps	Size C	Document Number SCH-27749 / PDF: SPF-27749	Rev E
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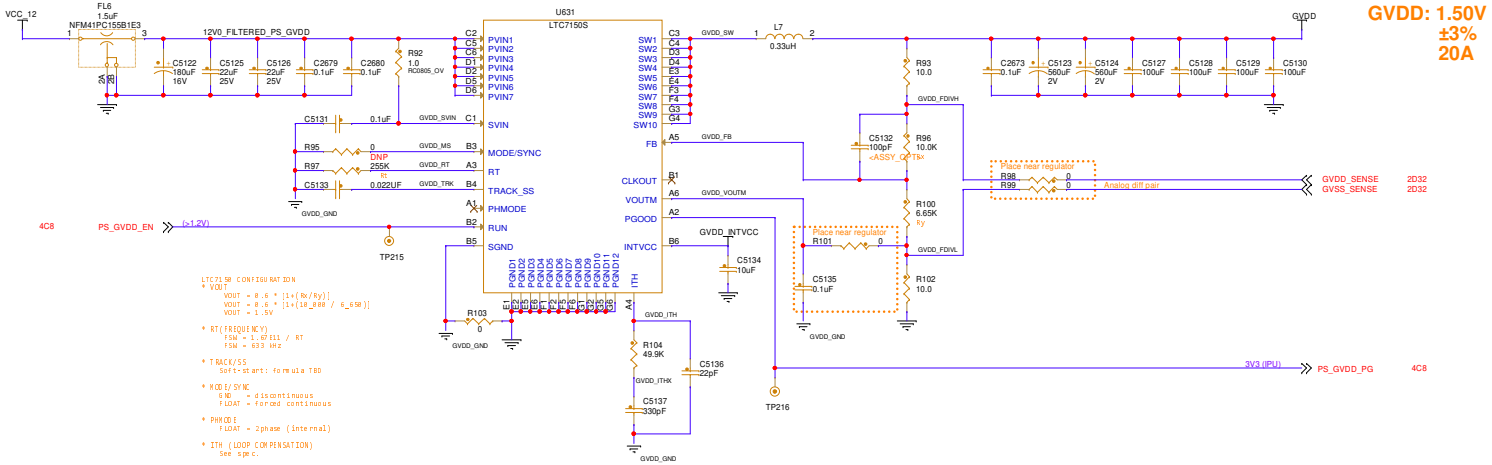
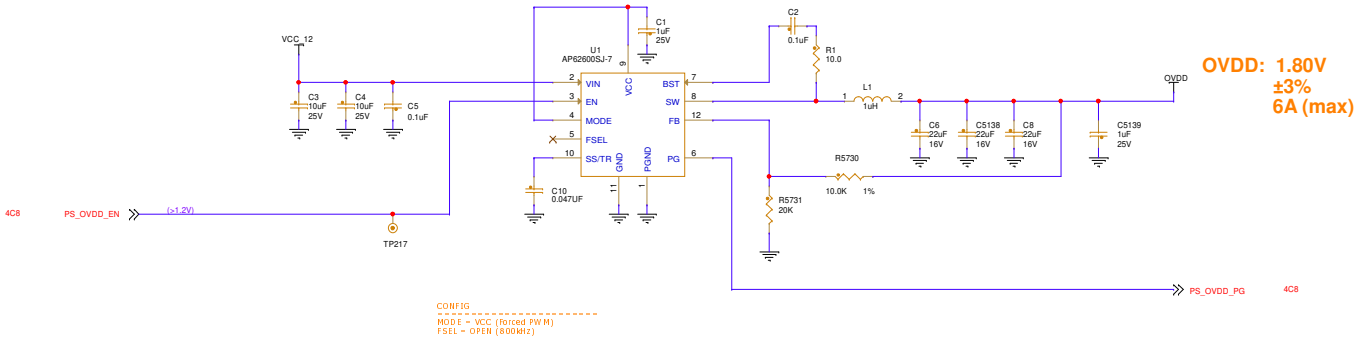
GVDD & OVDD POWER





NOTE: Could be replaced with AP64501 @ 5A (sufficient) which is qual'd for -40-125C

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Drawn by: GMillorn	Page Title: GVDD and OVDD/1V8 Power		
Approved: DN_Apps	Size C	Document Number SCH-27749 / PDF: SPF-27749	Rev E
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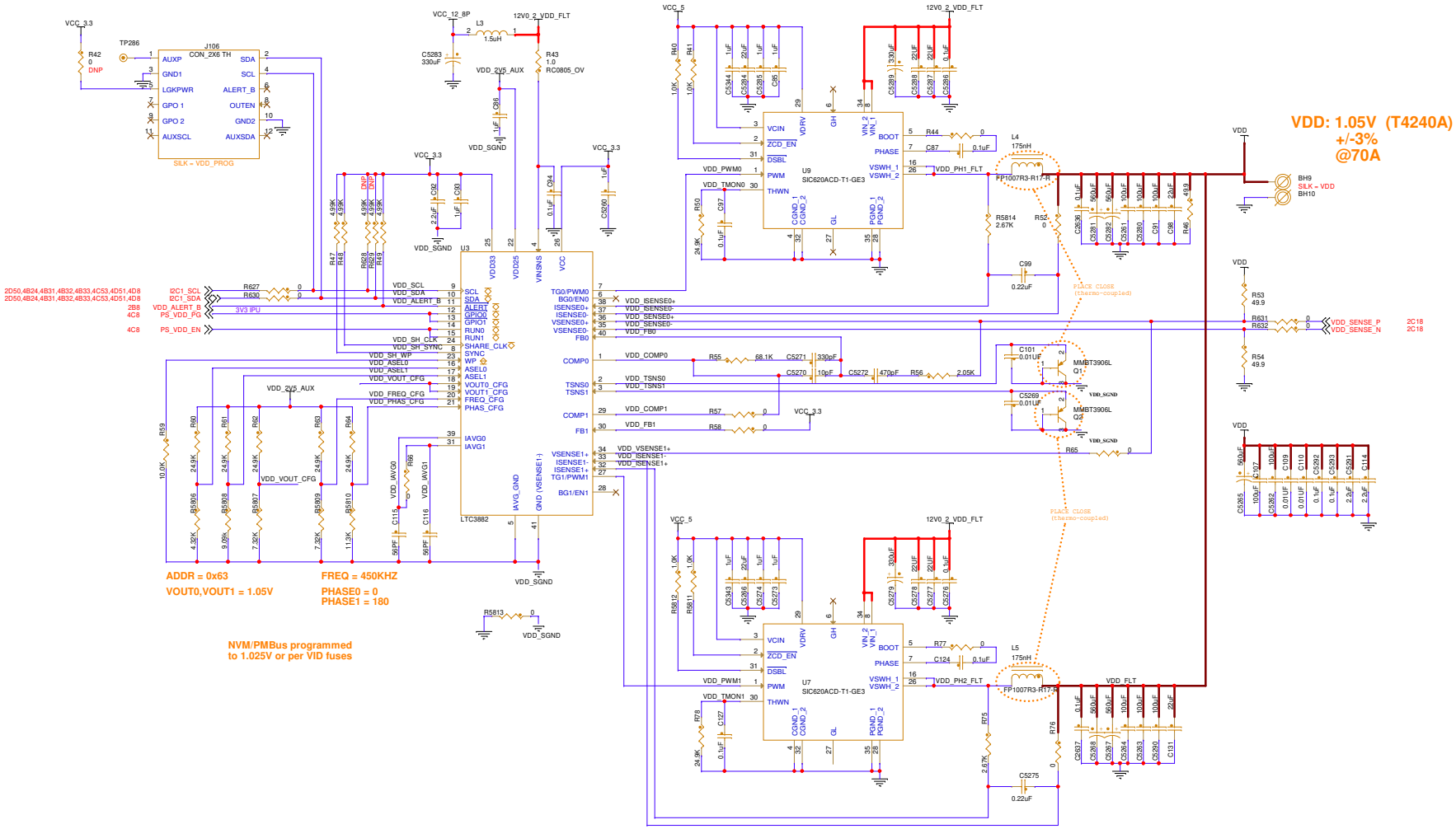
VDD POWER



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Approved: DN_Apps	Size C	Document Number SCH-27749 / PDF: SPF-27749	Rev E
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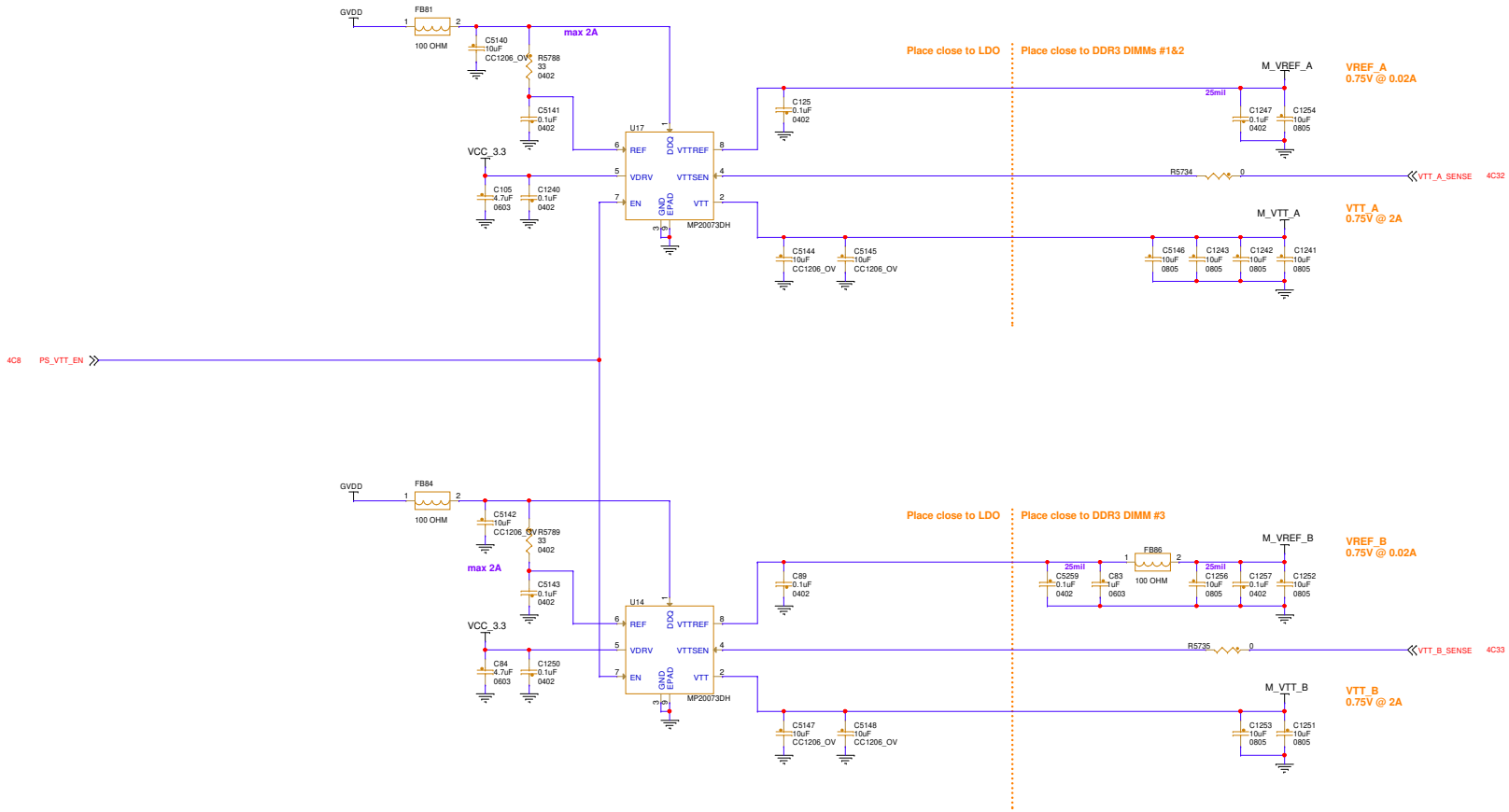
DDR VTT+MVREF POWER



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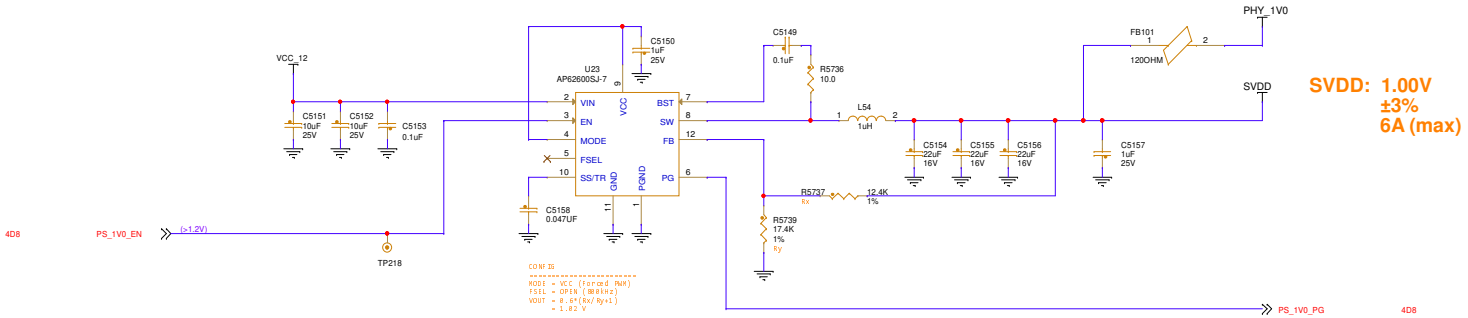
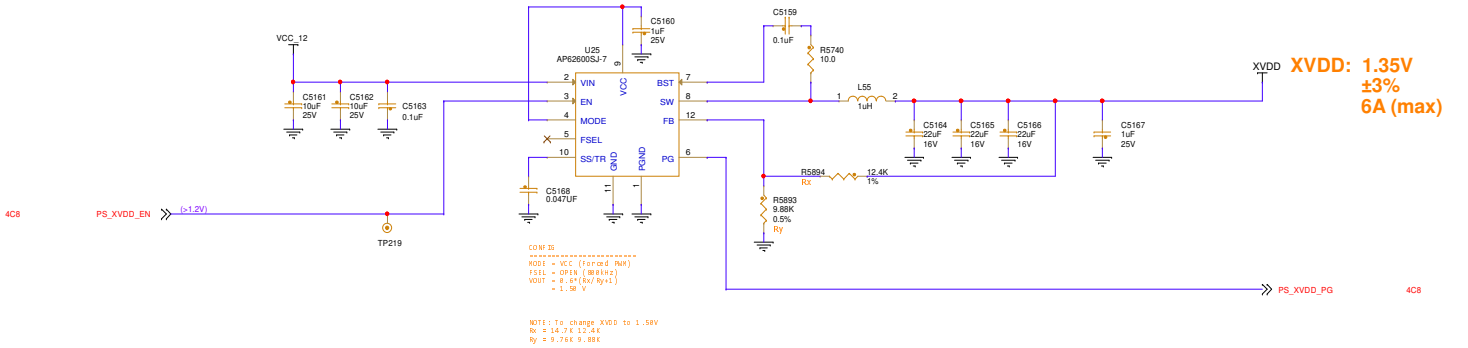
Drawn by: GMillorn	Page Title: DDR VTT+MVREF Power		
Approved: DN_Apps	Size C	Document Number SCH-27749 / PDF: SPF-27749	Rev E
	Date: Tuesday, November 21, 2023	Sheet 13 of 55	

SVDD & XVDD POWER



SVDD: 1.00V ±3% 6A (max)



XVDD: 1.35V ±3% 6A (max)

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Drawn by: GMillorn	Page Title: SVDD & XVDD Power		
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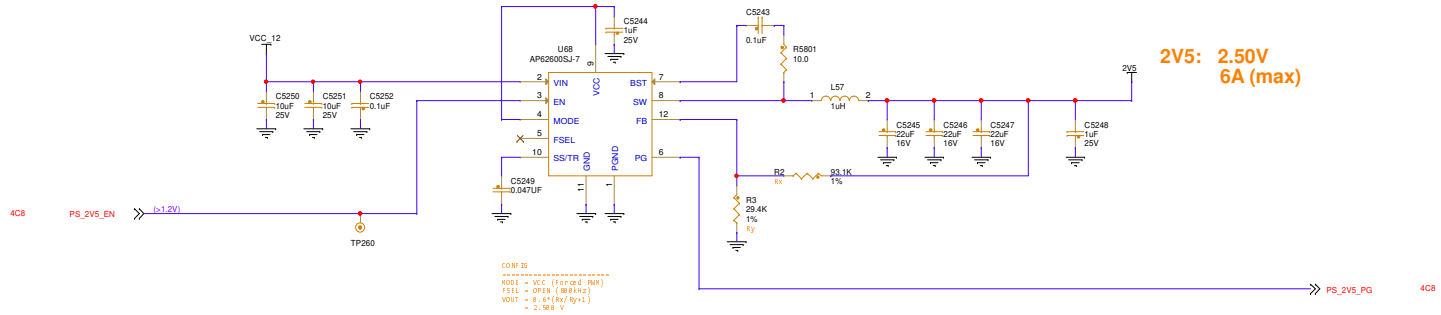
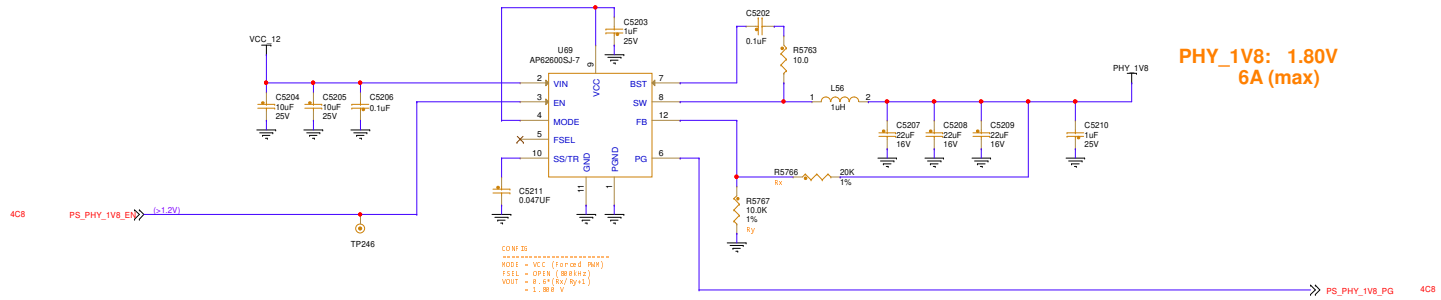
2V5 & PHY 1V8 POWER



2V5: 2.50V
6A (max)



PHY_1V8: 1.80V
6A (max)

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Approved: DN_Apps	Size C	Document Number SCH-27749 / PDF: SPF-27749	Rev E
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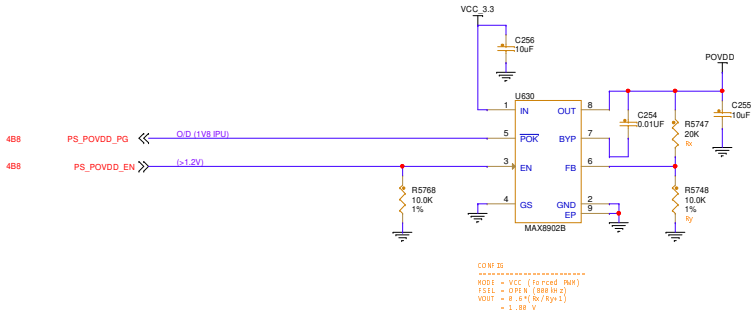
MISC POWER



POVDD: 1.80V @ 0.5A (max)
Only on for fuse programming.

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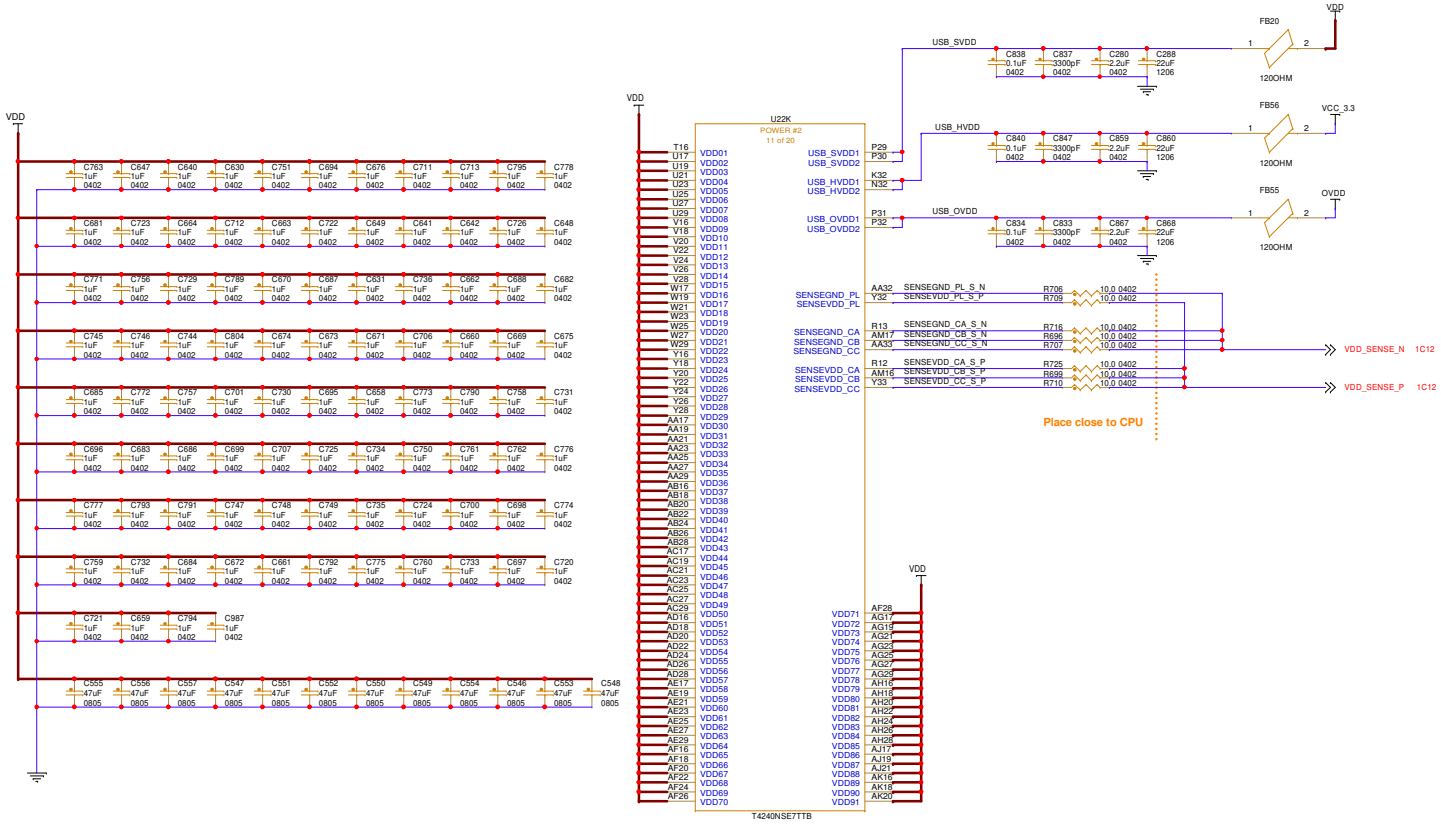
T4240 VDD/CORE POWER



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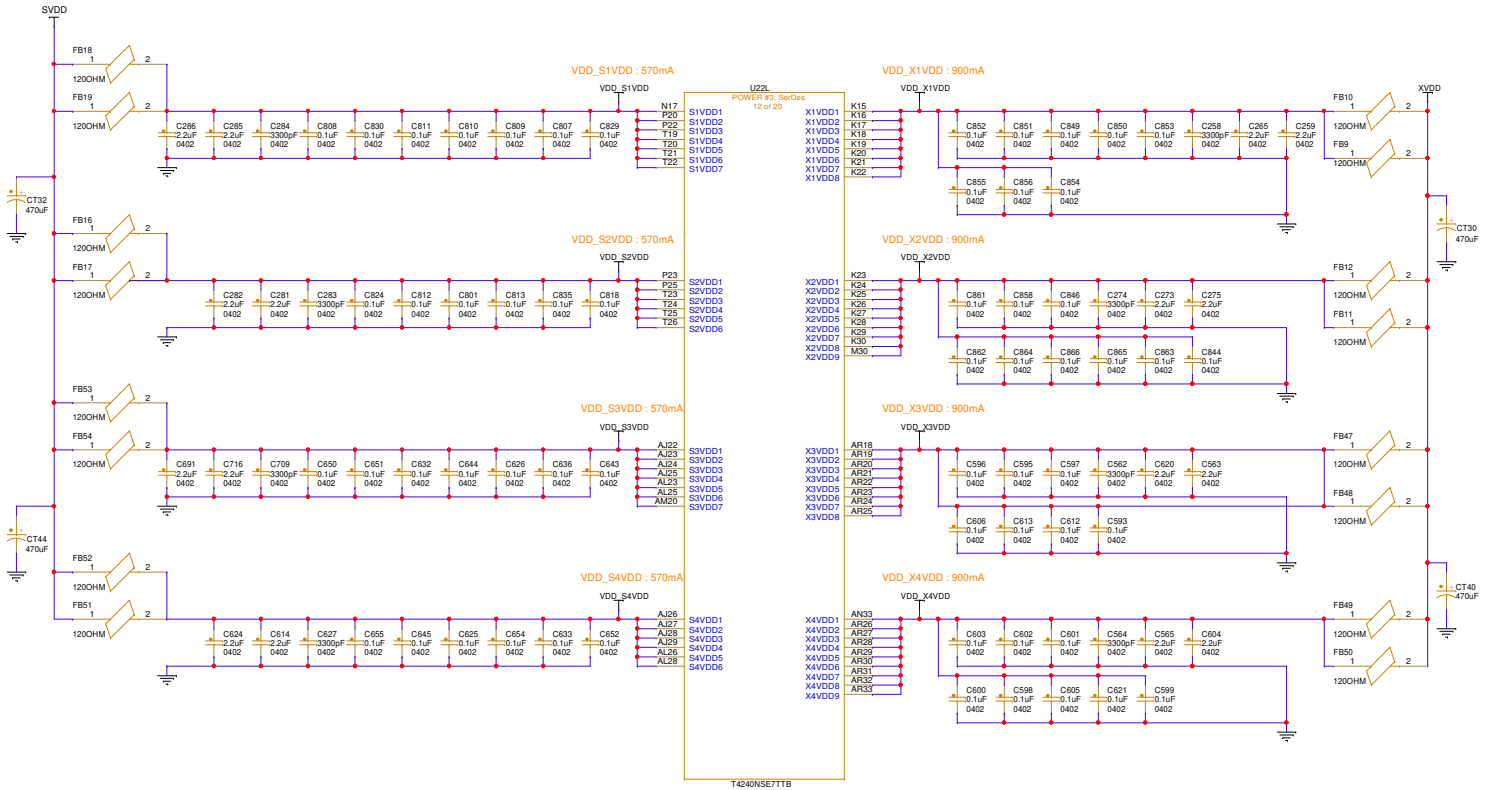
T4240 SVDD / XVDD POWER



NOTE: Power supplied by paralleled filters to lower I-R drop.

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Approved: DN_Apps	Size C	Document Number SCH-27749 / PDF: SPF-27749	Rev E
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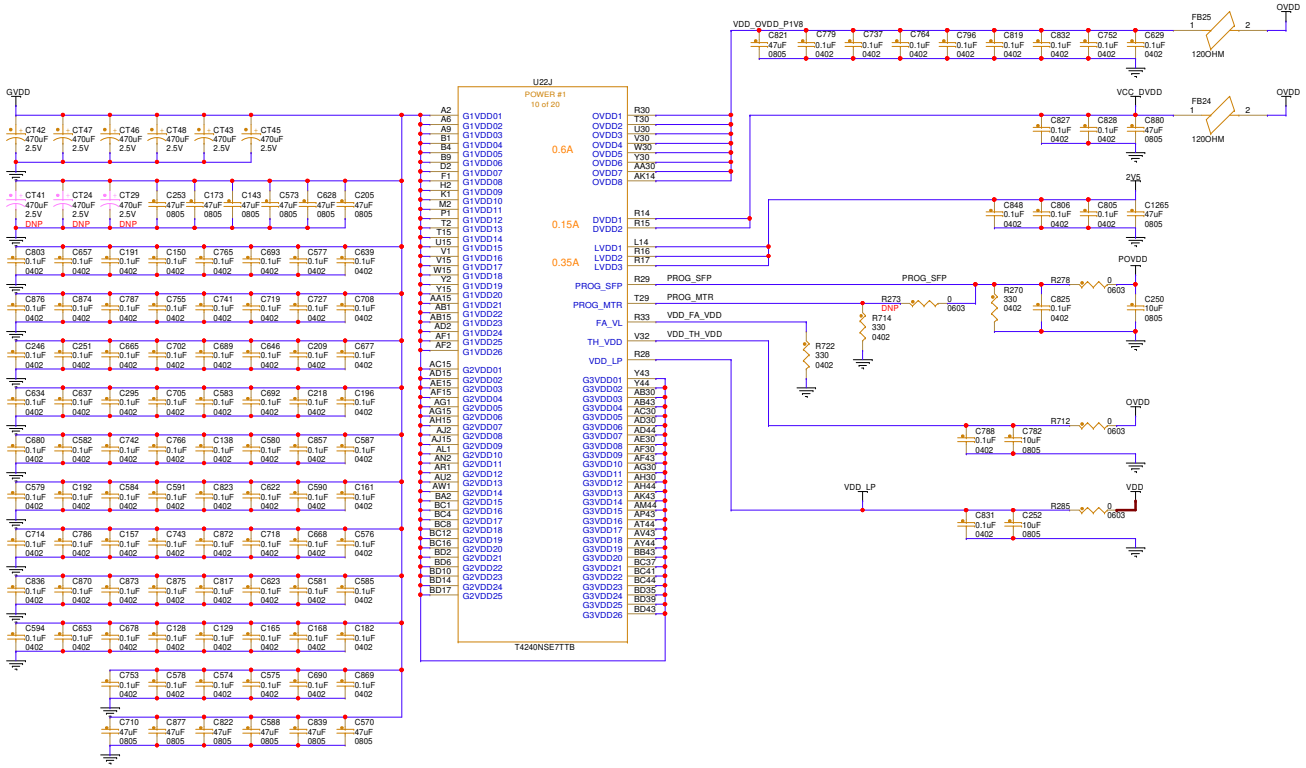
T4240 GVDD / Other Power



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Approved: DN_Apps	Size C	Document Number SCH-27749 / PDF: SPF-27749	Rev E
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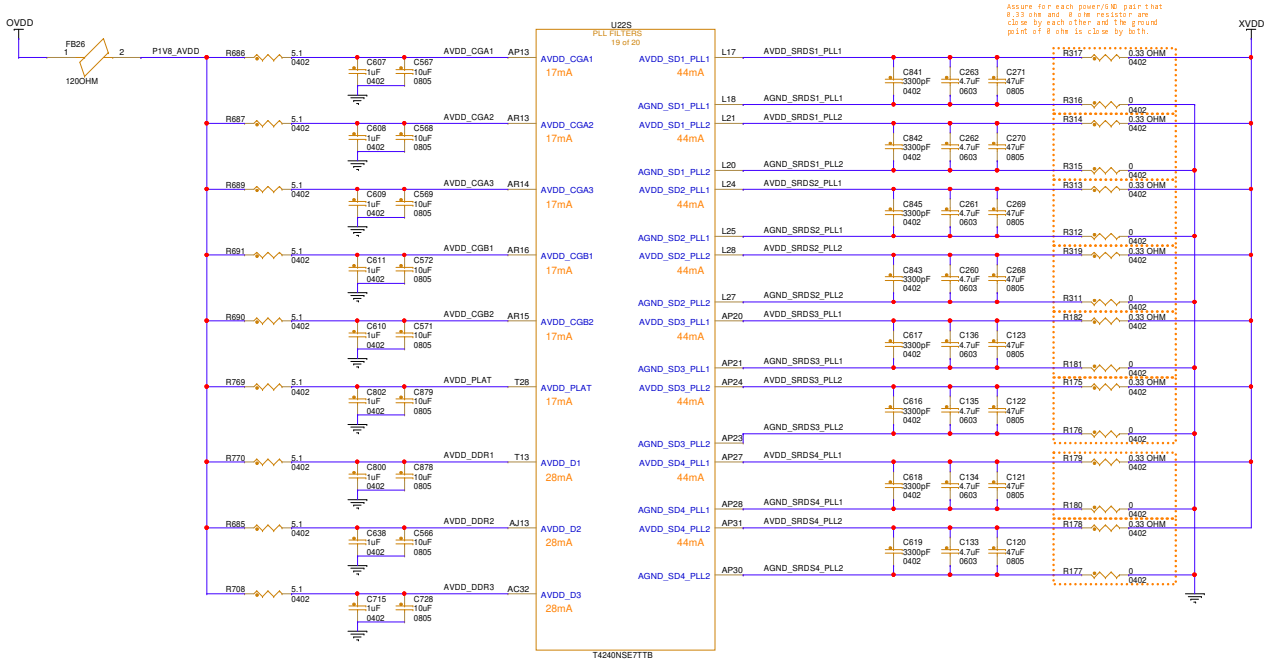
T4240 PLL Filters



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Approved: DN_Apps	Size C	Document Number SCH-27749 / PDF: SPF-27749	Rev E
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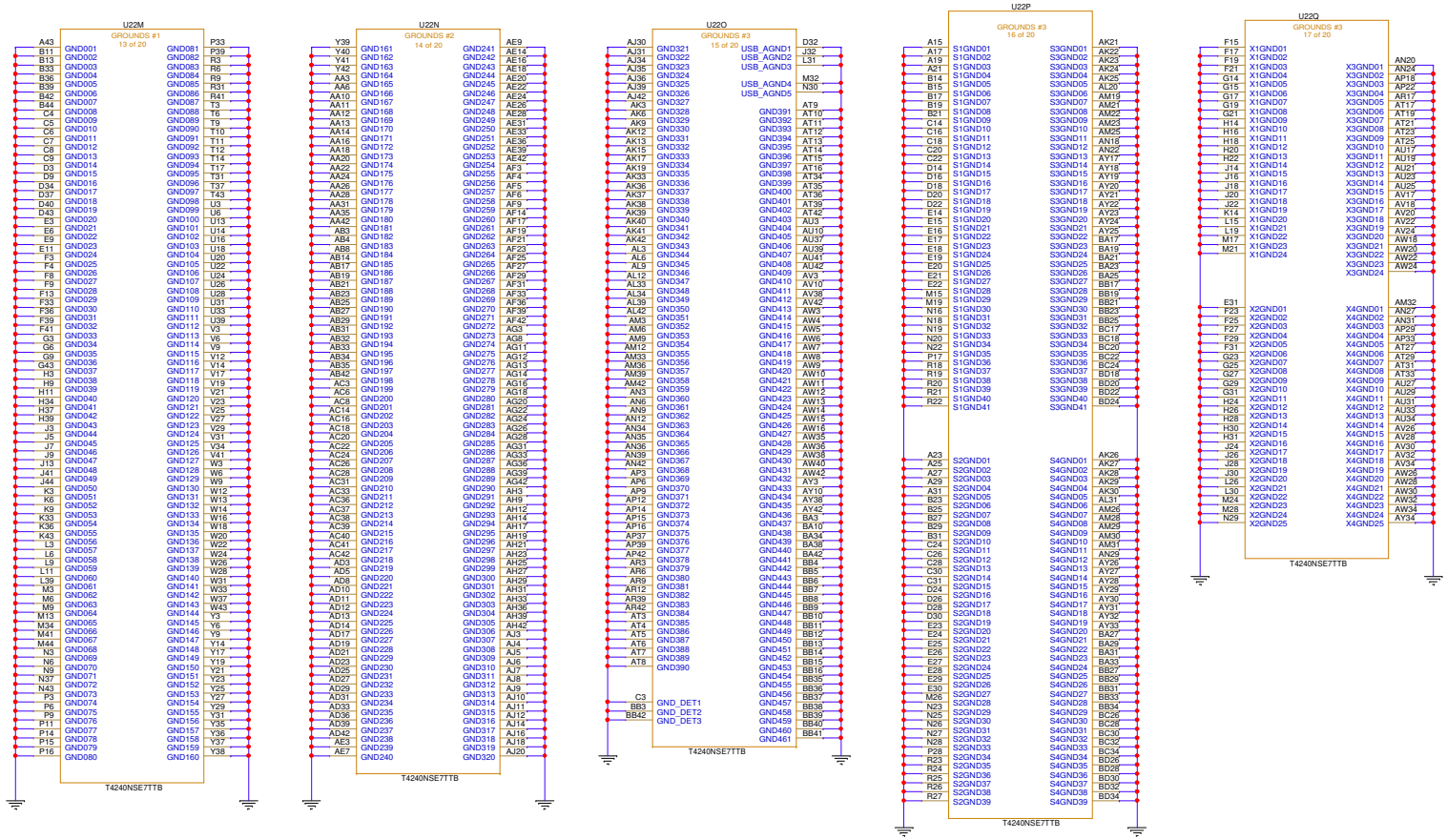
T4240 Ground Pins



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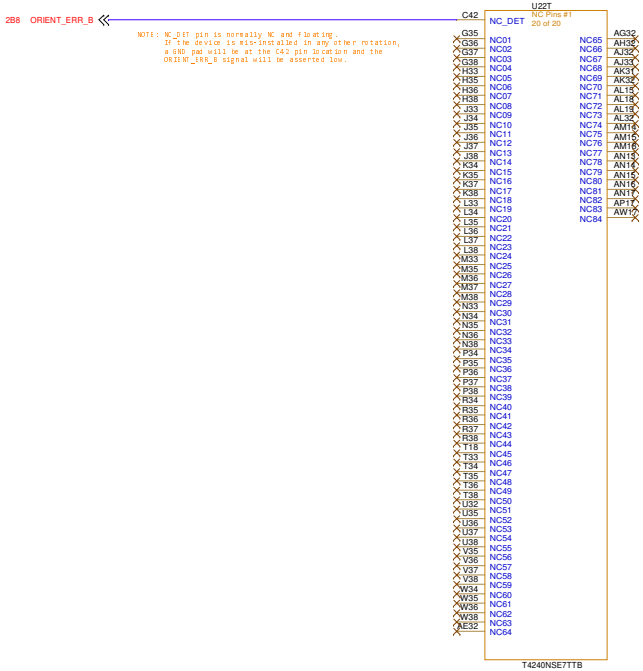
T4240 NC Pins



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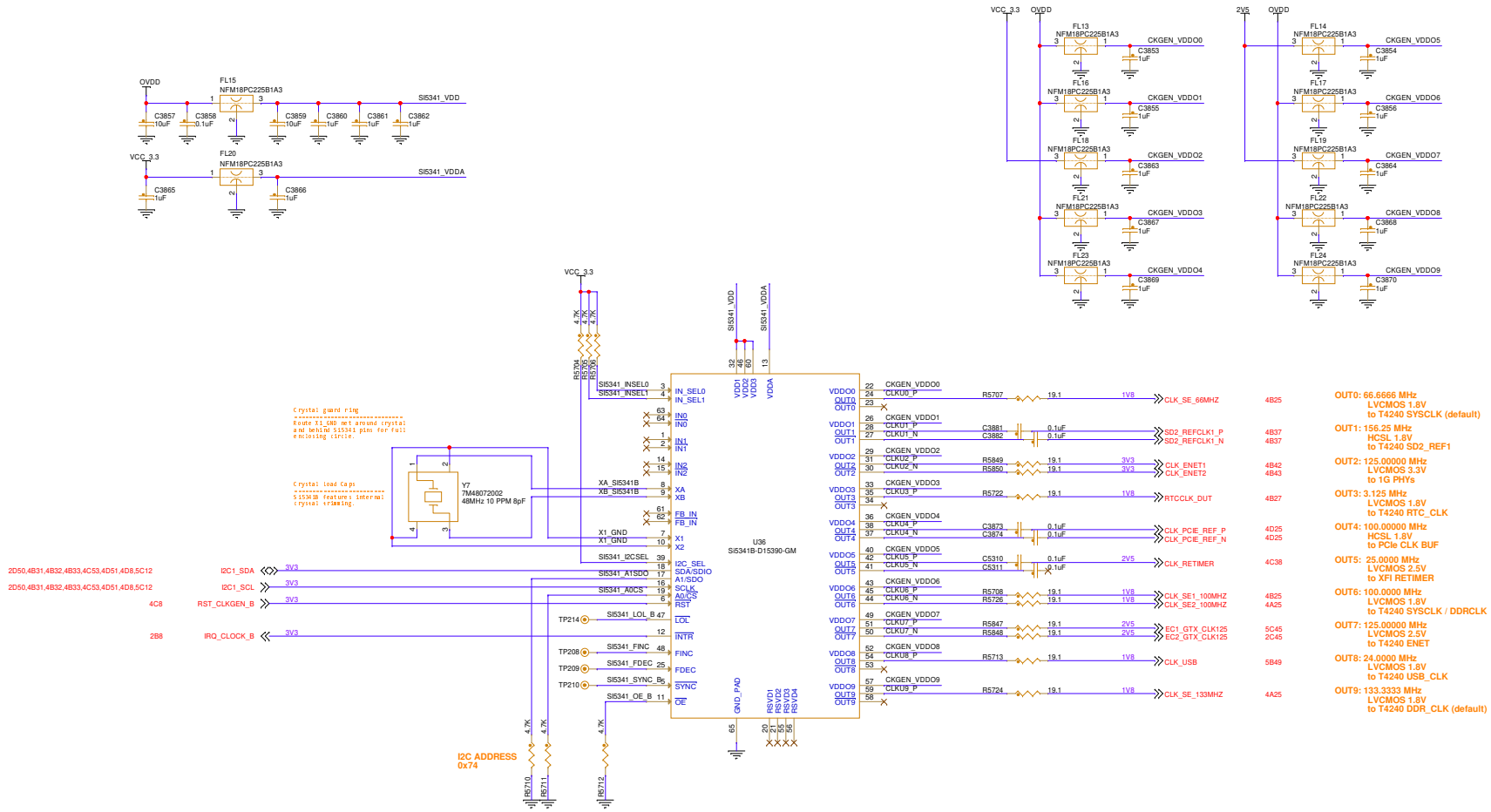
SYSCLK / DDRCLK / REF Clocks



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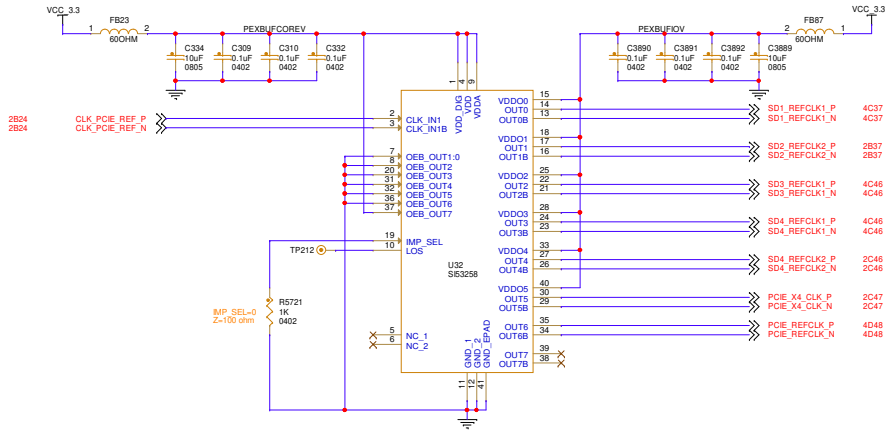
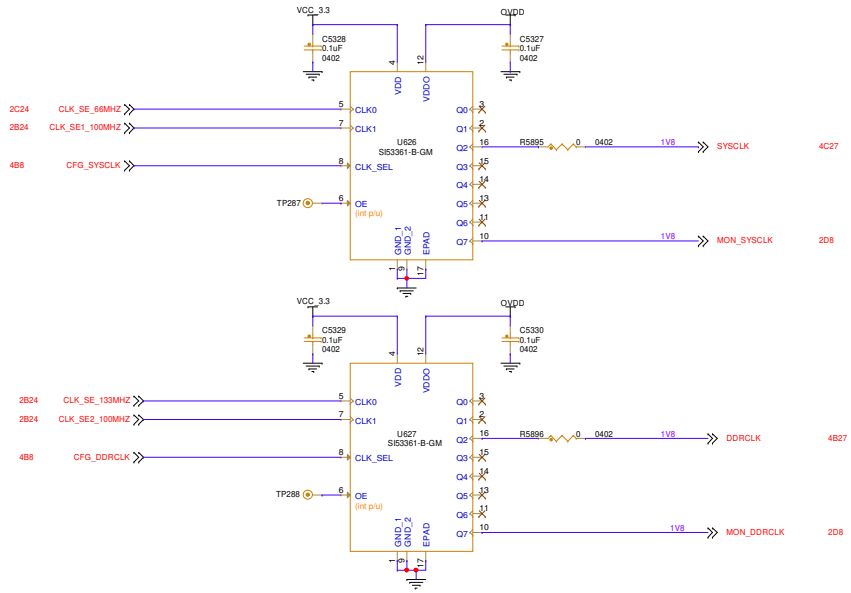
PCIe Clock Buffers



DUT Clock Select



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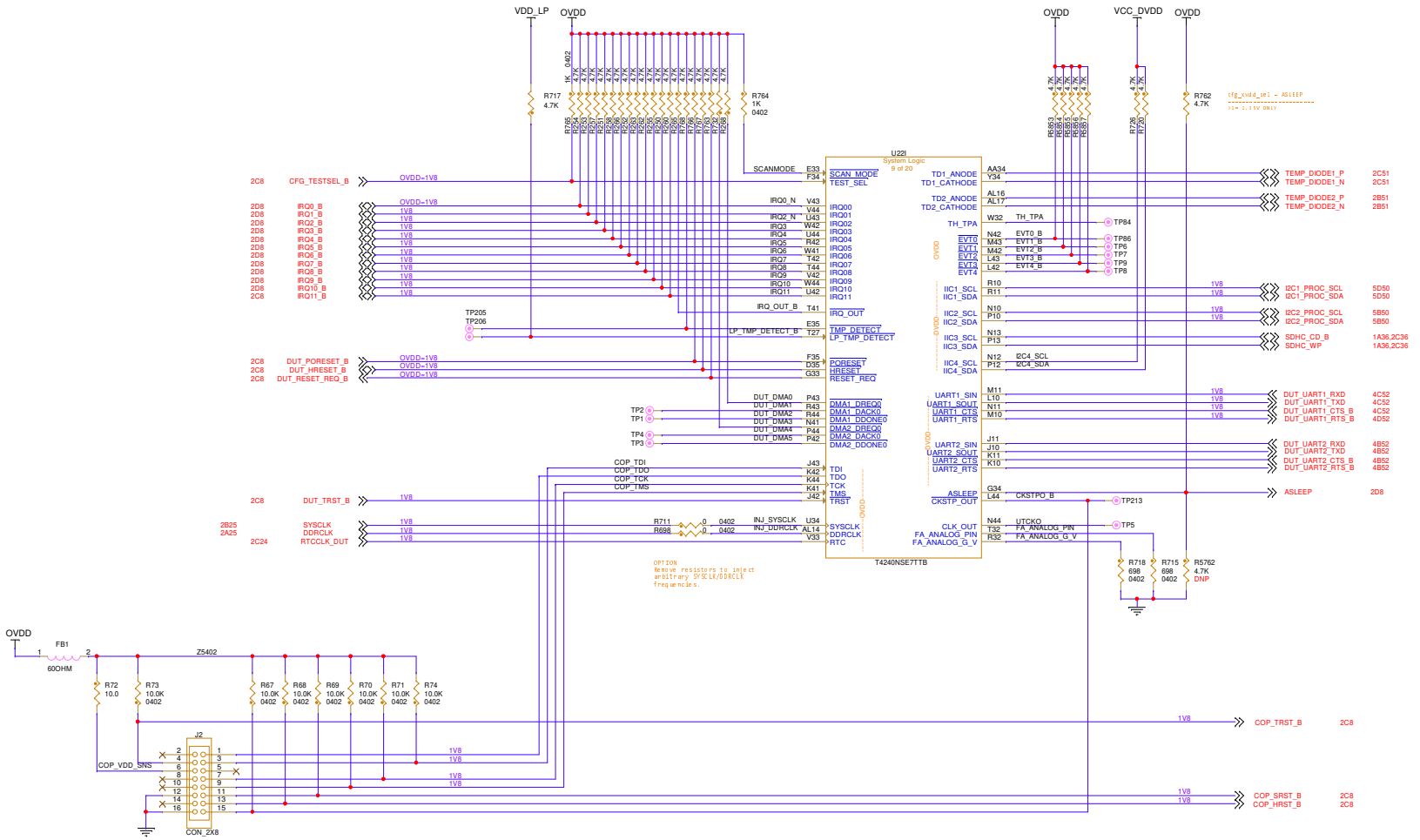
T4240 System Block & COP



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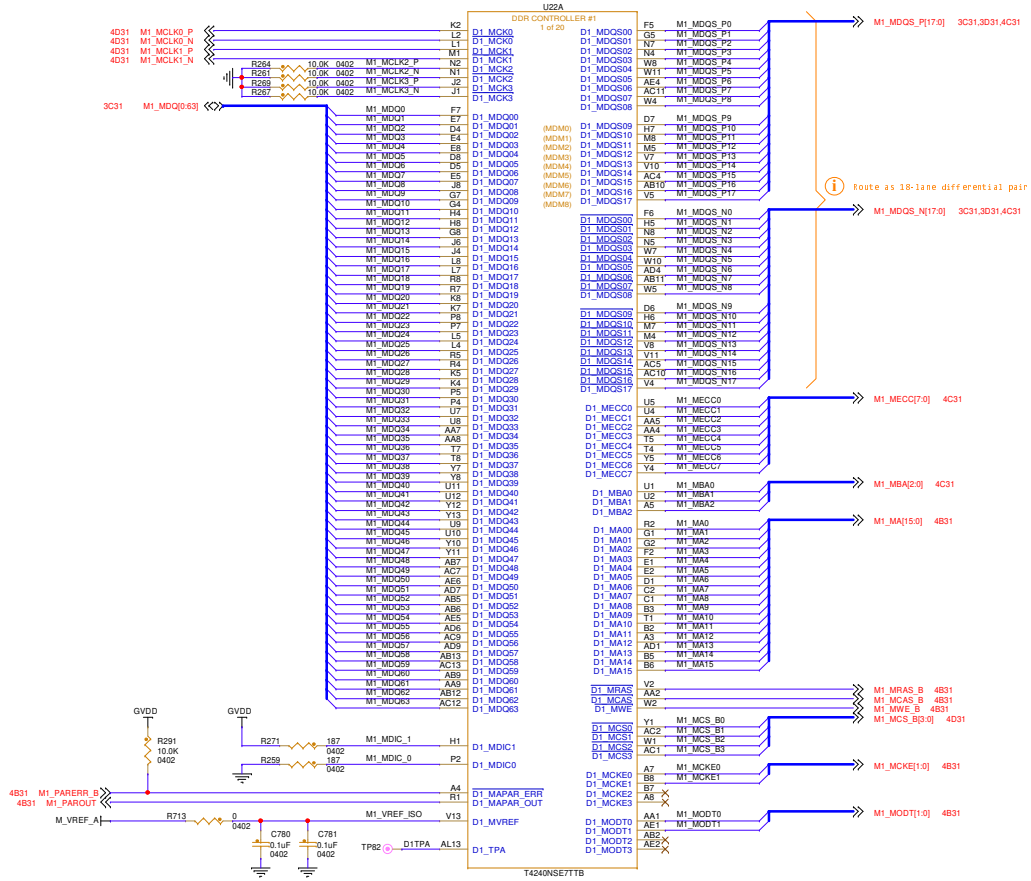
T4240 DDR Port #1



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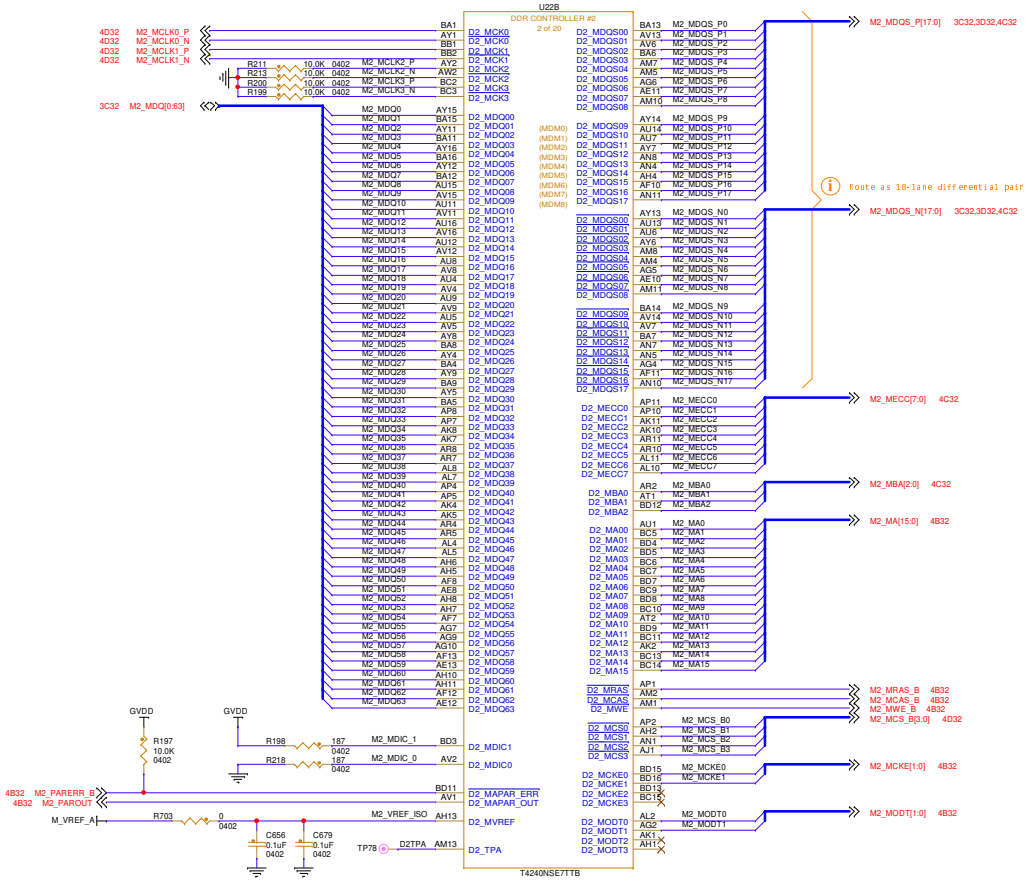
T4240 DDR Port #2



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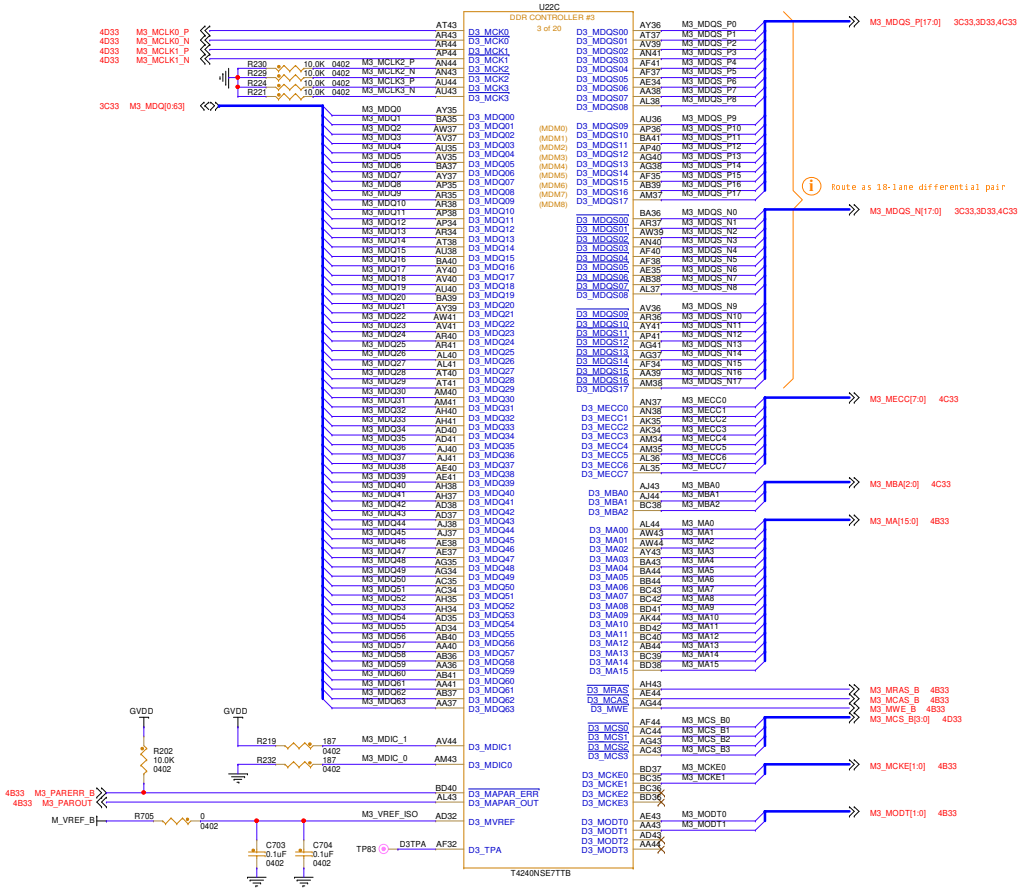
T4240 DDR Port #3



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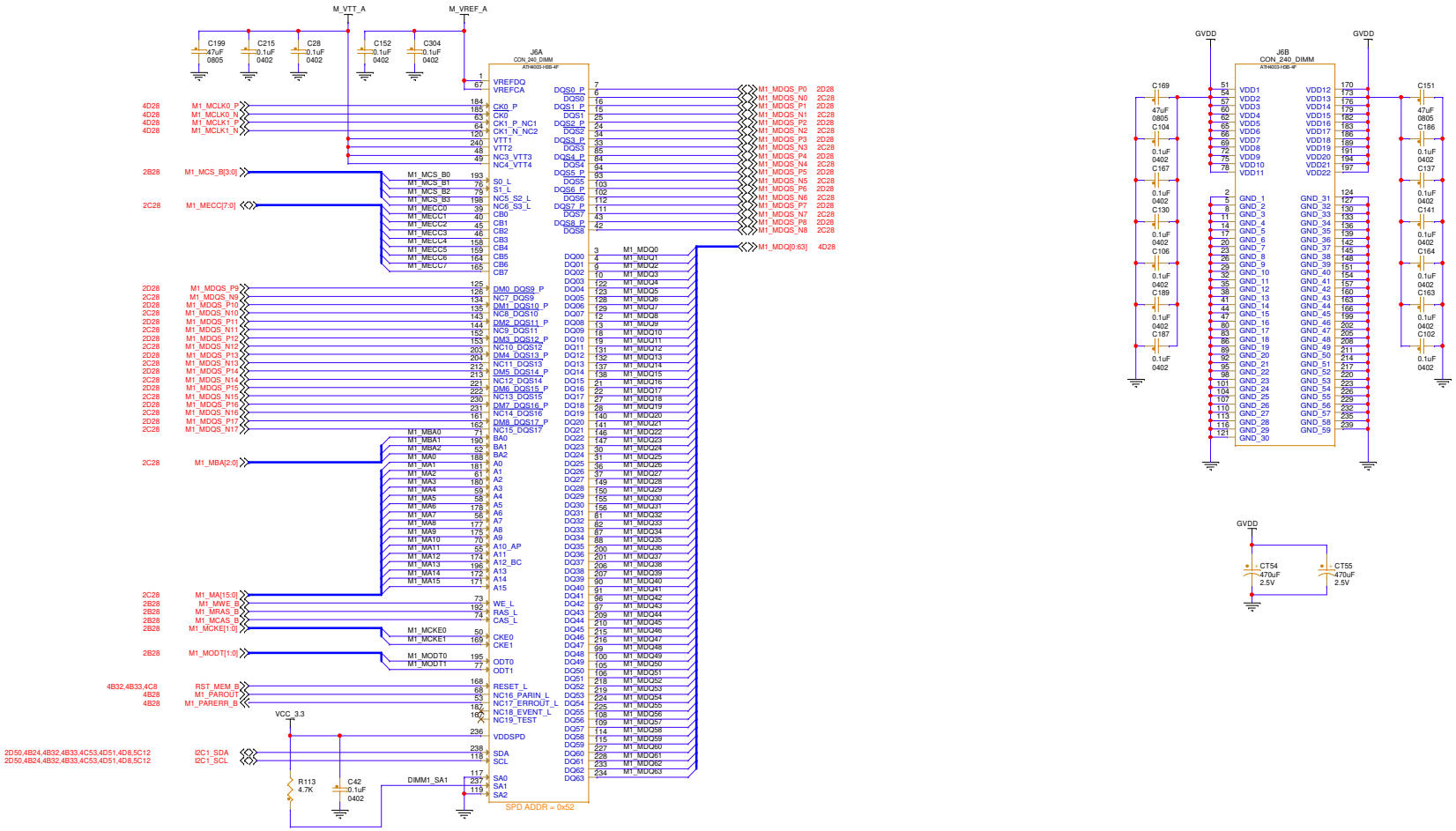
DDR3 DIMM #1



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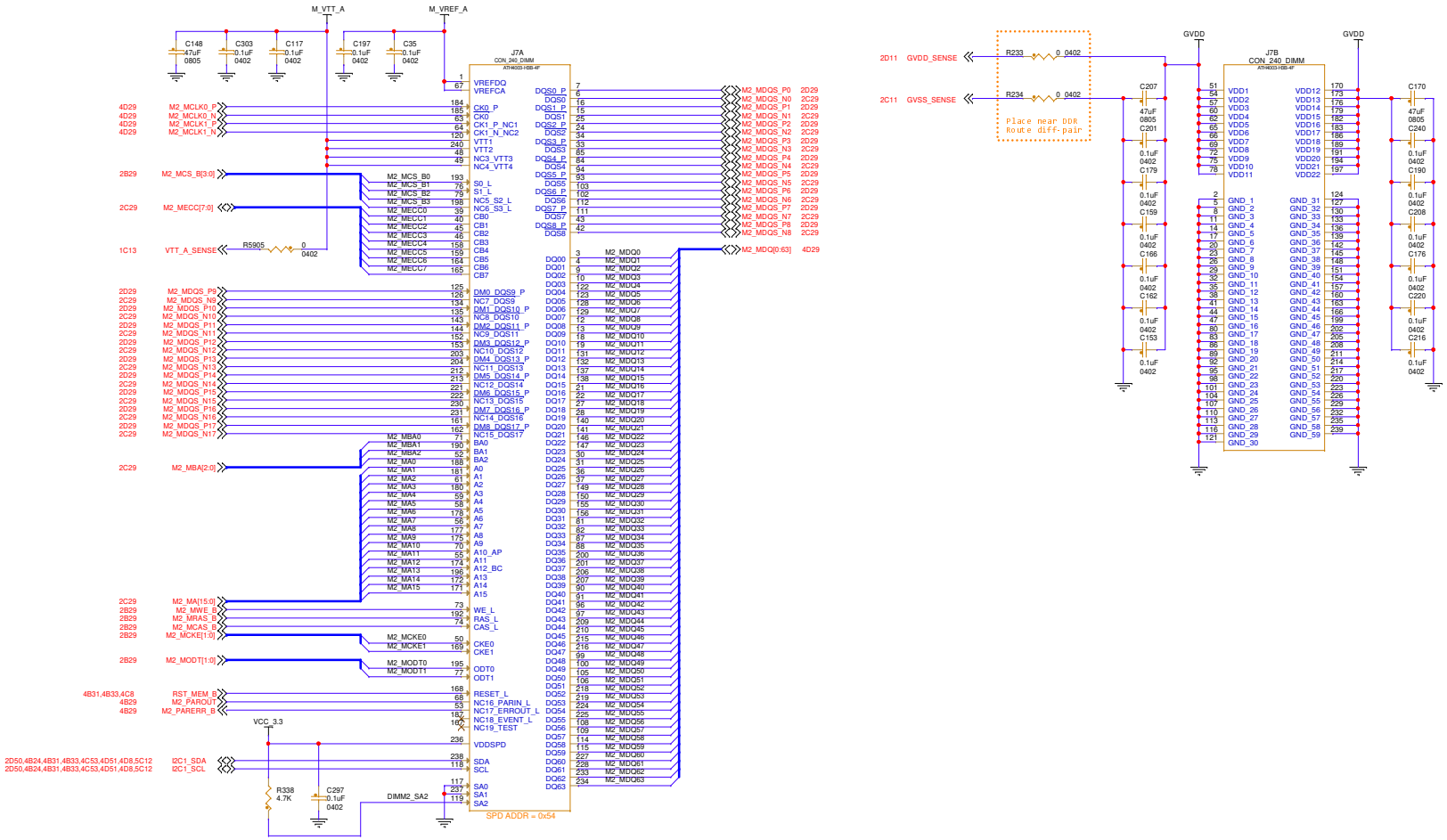
DDR3 DIMM #2



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Approved: DN_Apps	Size C	Document Number SCH-27749 / PDF: SPF-27749	Rev E
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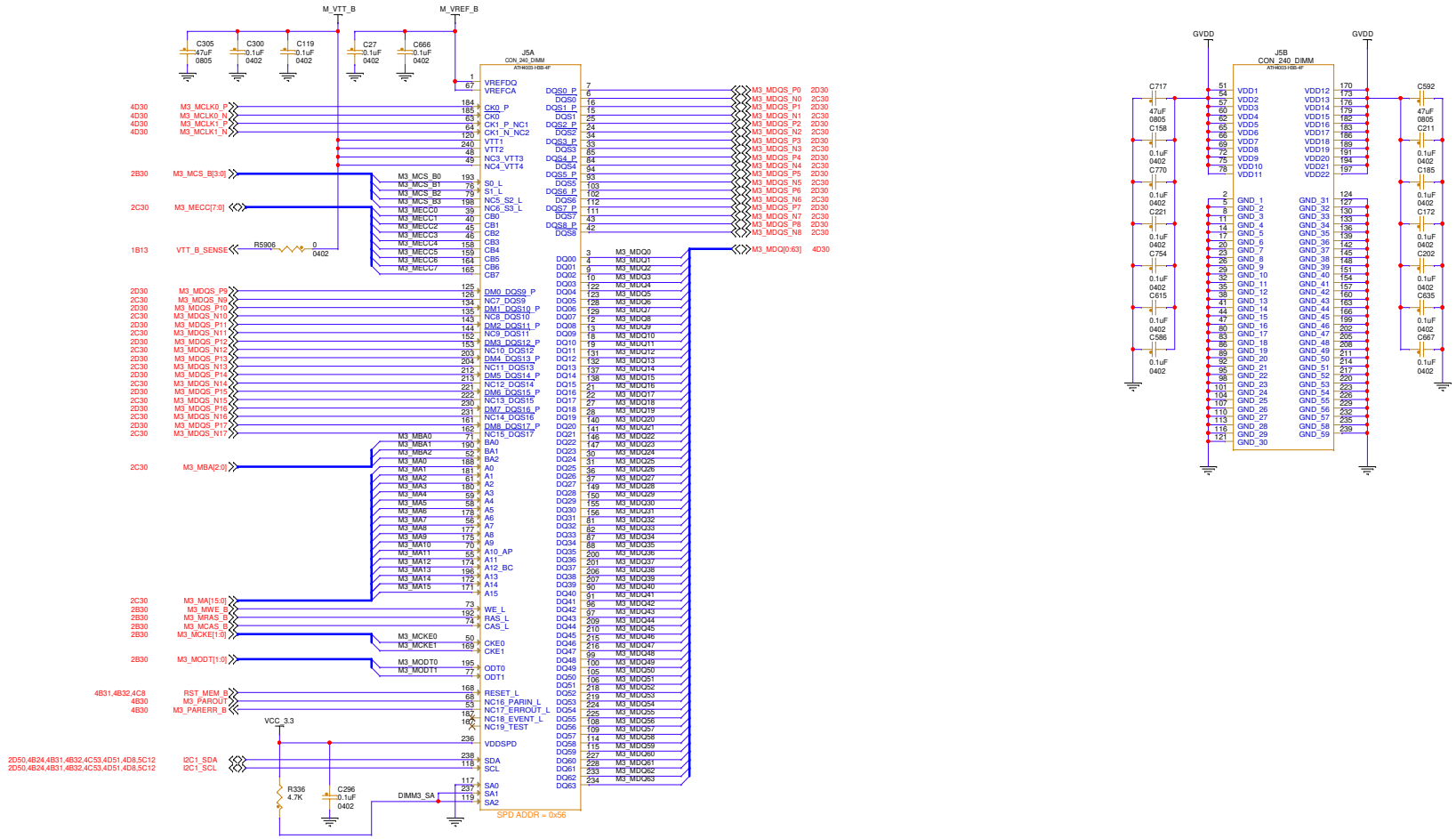
DDR3 DIMM #3



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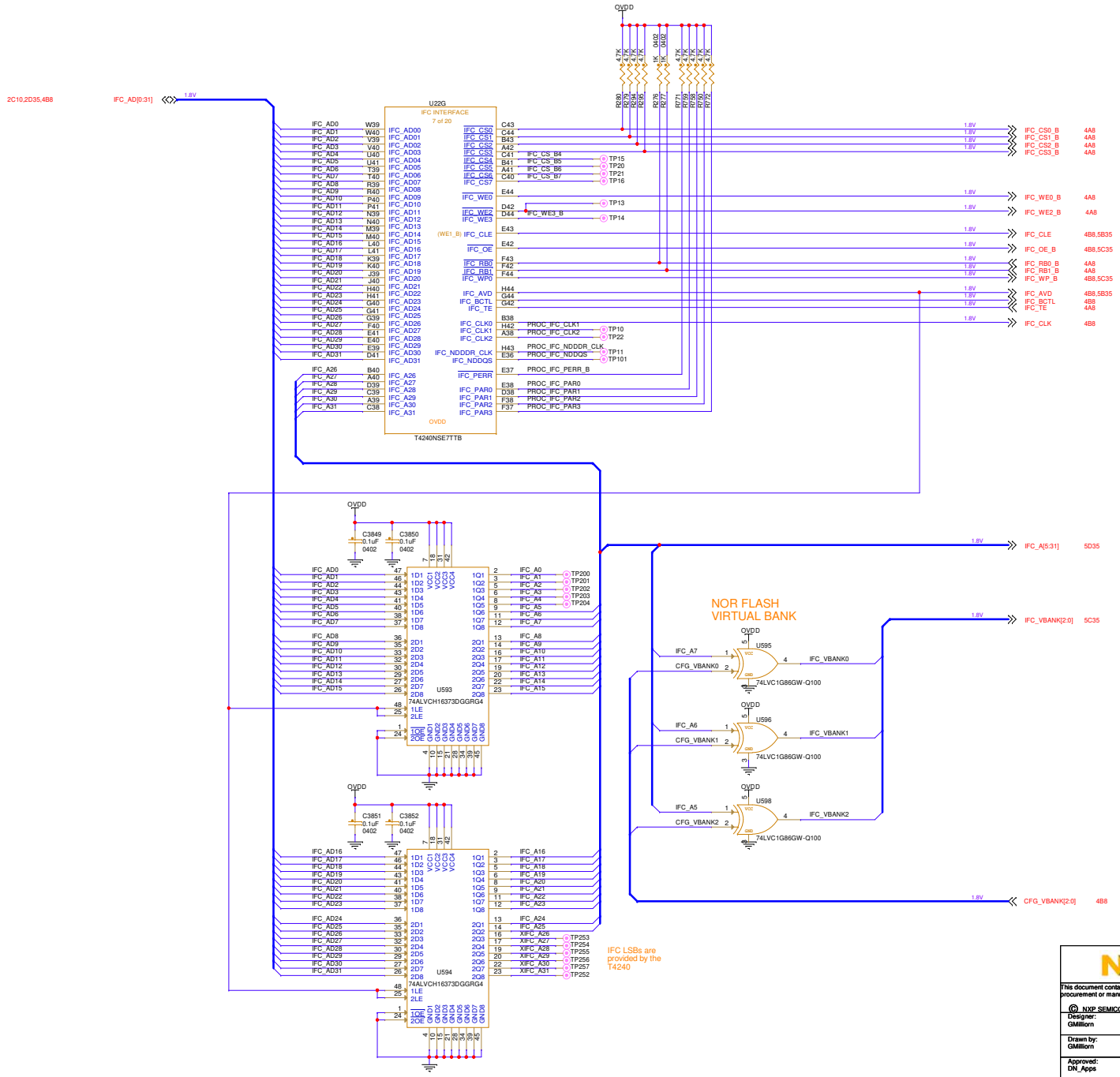
T4240 IFC Interface



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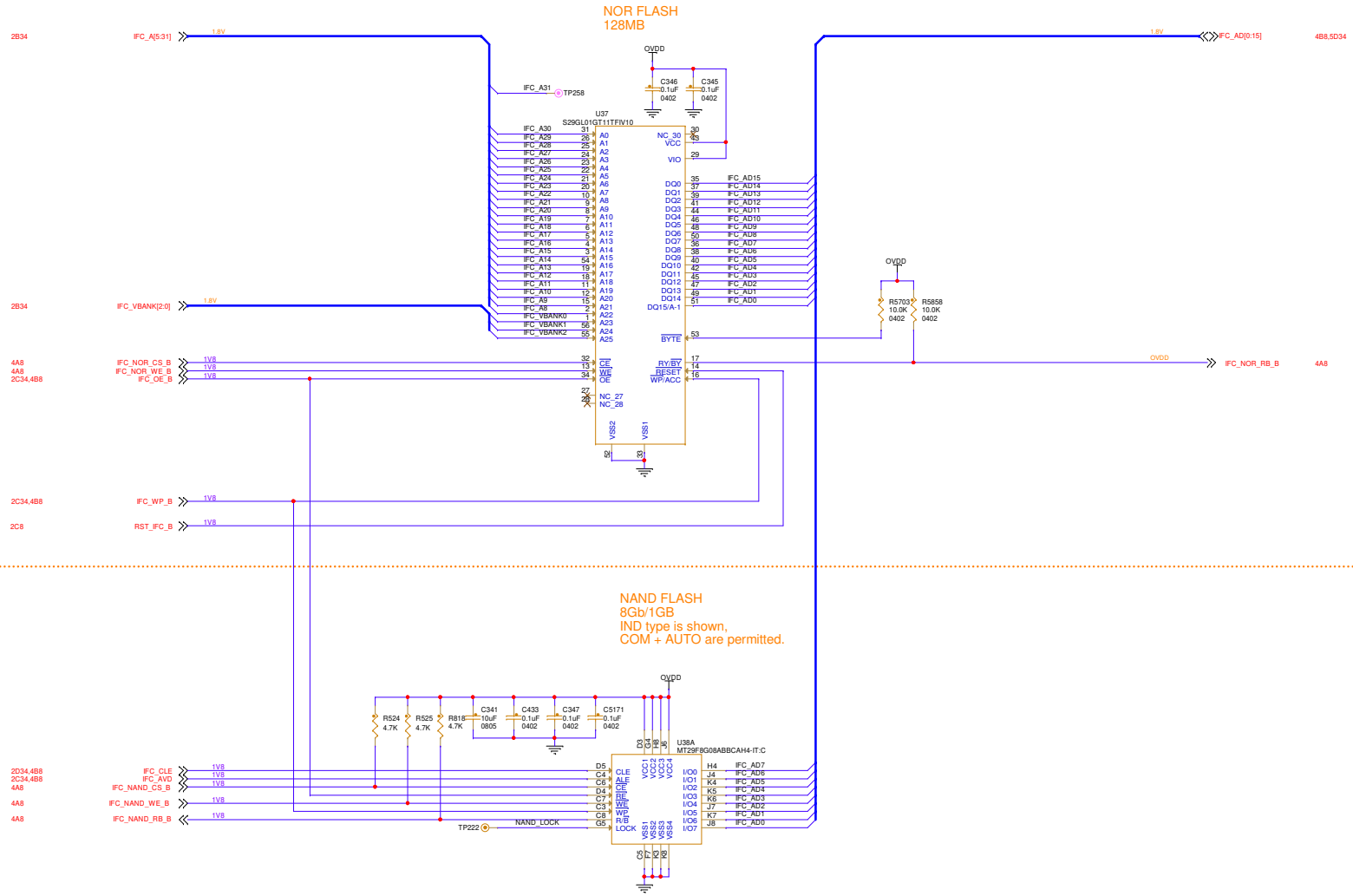
NOR & NAND Flash



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Approved: DN_Apps	Size C	Document Number SCH-27749 / PDF: SPF-27749	Rev E
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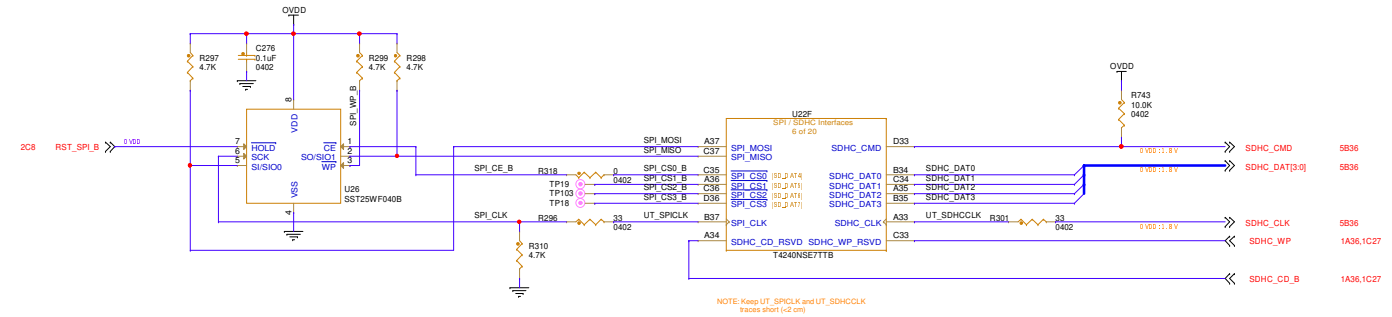
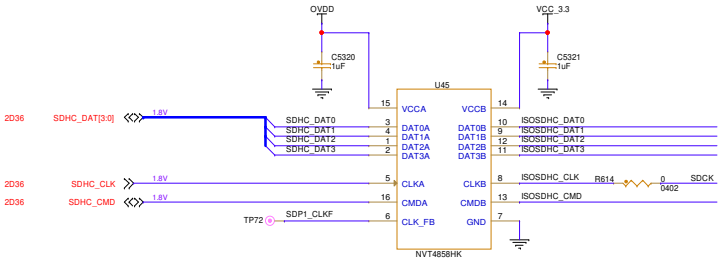
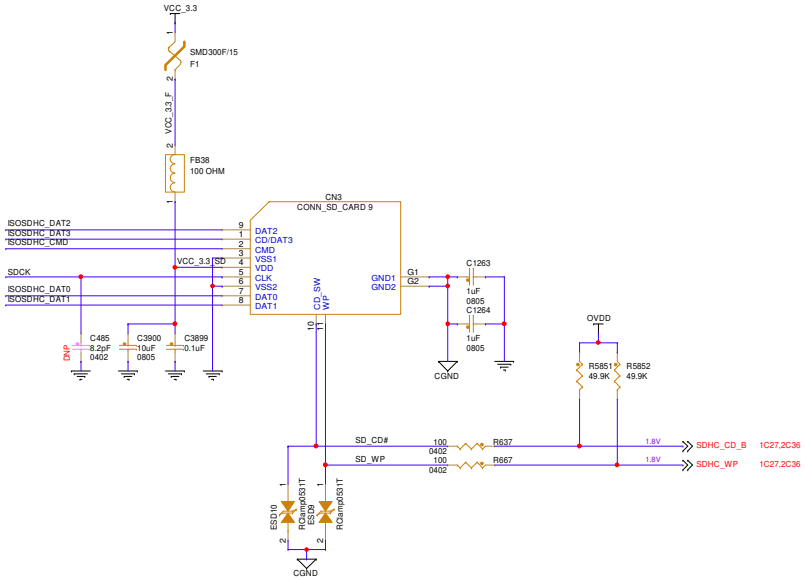
SPI & SD Card Interface







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FRONT SIDE SERDES 1 & 2 (ENET)

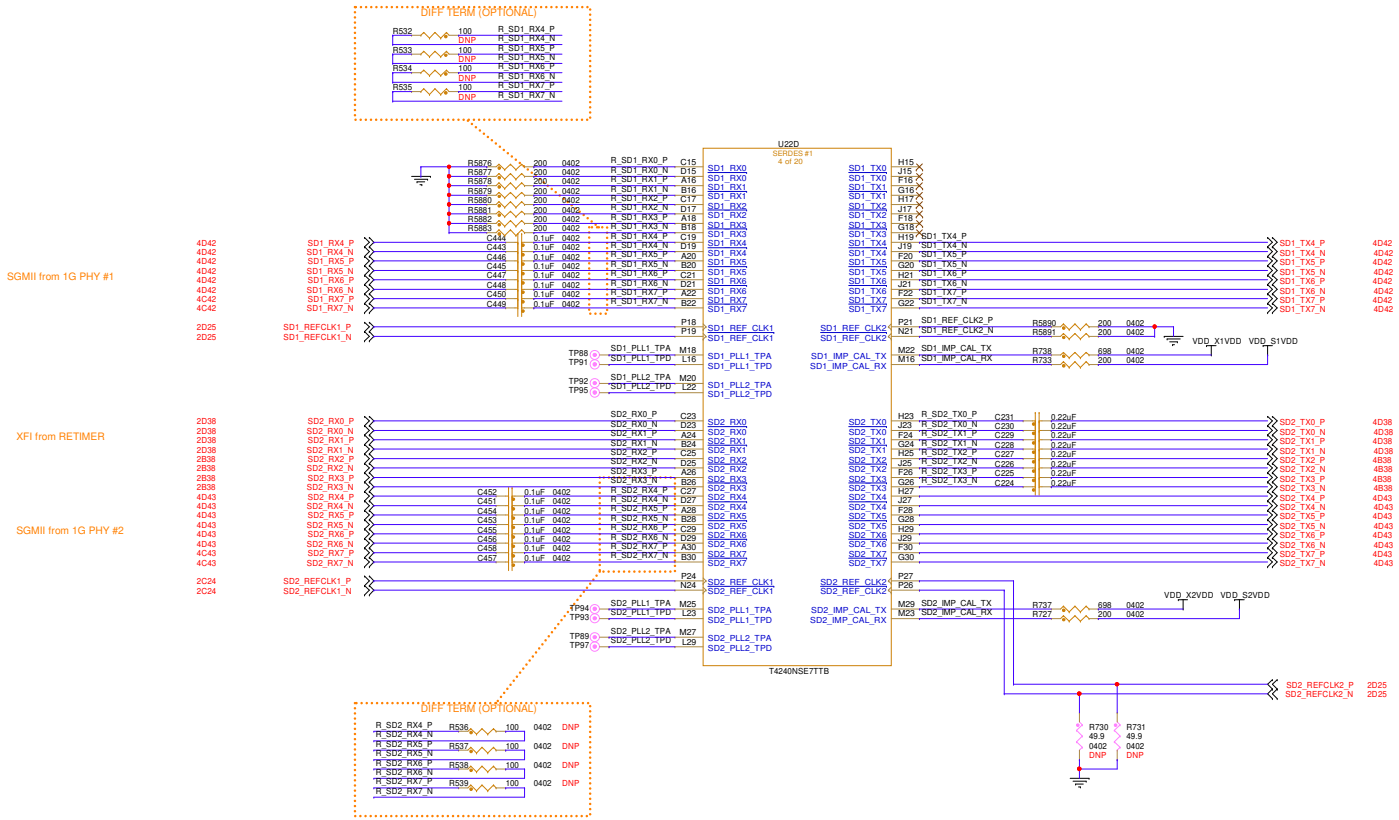

Table 18-1. SerDes 1

SRDS_PRTCL_S1			SerDes 1								
Decimal	Hex	ECI(RGMII)	A	B	C	D	E	F	G	H	Per Lane PLL mapping
27	1B	r.+	sg1.5	sg1.6	sg1.10	sg1.9	sg1.1	sg1.2	sg1.3	sg1.4	11111111
35	23	r.+	sg1.5	sg1.6	sg1.10	sg1.9	*sg1.1*	*sg1.2*	*sg1.3*	*sg1.4*	11112222
4	4	r.*	*HiGig[2]1.9 (3.75)*				*HiGig[2]1.10 (3.75)*				11111111

Table 18-2. SerDes 2

SRDS_PRTCL_S2			SerDes 2								
Decimal	Hex	ECI(RGMII)	A	B	C	D	E	F	G	H	Per Lane PLL mapping
55	37	r2.5	XFI1.9	XFI1.10	XFI2.10	XFI2.9	sg2.1	sg2.2	sg2.3	sg2.4	11112222
57	39	r2.5	XFI1.9	XFI1.10	XFI2.10	XFI2.9	*sg2.1*	*sg2.2*	*sg2.3*	*sg2.4*	11112222

```
SerDes 1 configuration
==================================================
RCW[SRDS_PRTCL_S1]=            7 - Unused x4 & 1 G PHY
PLL mapping=                   11111111
RCW[SRDS_PLL_PD_S1]=           01
RCW[SRDS_PLL_REF_CLK_SEL_S1]= 0: PLL1=100MHz
```

```
SerDes 2 configuration
==================================================
RCW[SRDS_PRTCL_S2]=            55 - XFI & 1 G PHY
PLL mapping=                   11112222
RCW[SRDS_PLL_PD_S2]=           00
RCW[SRDS_PLL_REF_CLK_SEL_S2]= 0: PLL1=156.25MHZ & PLL2=100MHz
```


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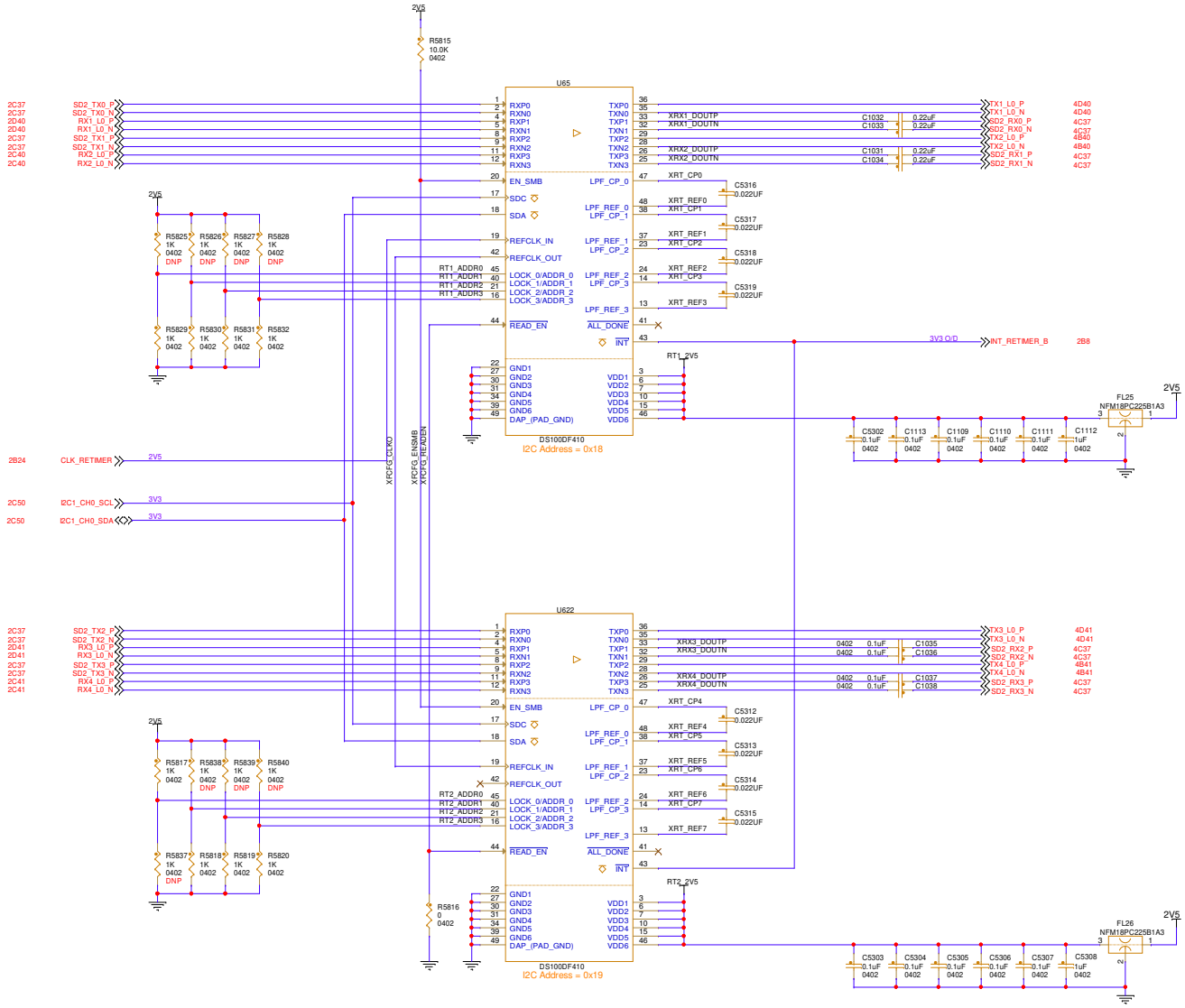
10GE: XFI/SFP Retimer



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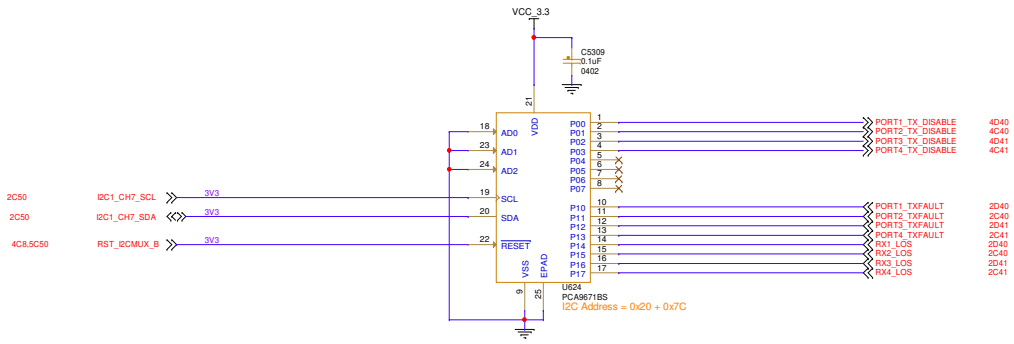
SFP Monitor/Control



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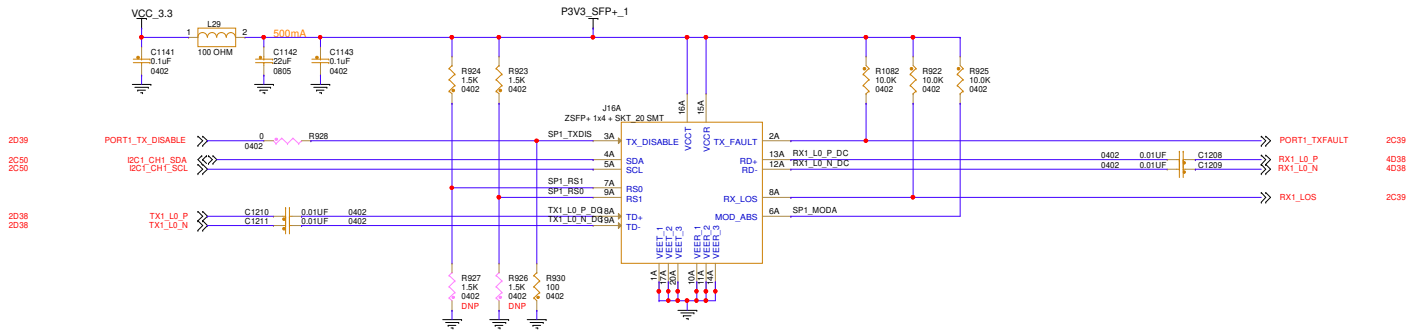
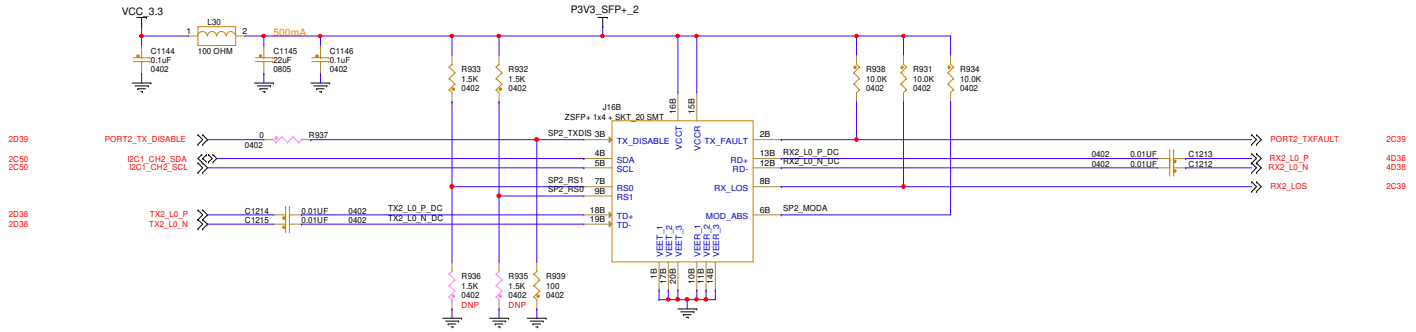
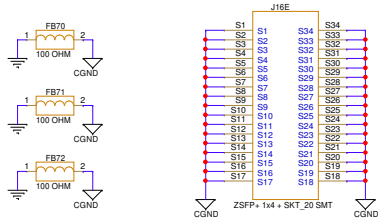
SFP Ports 1 / 2 / Cage







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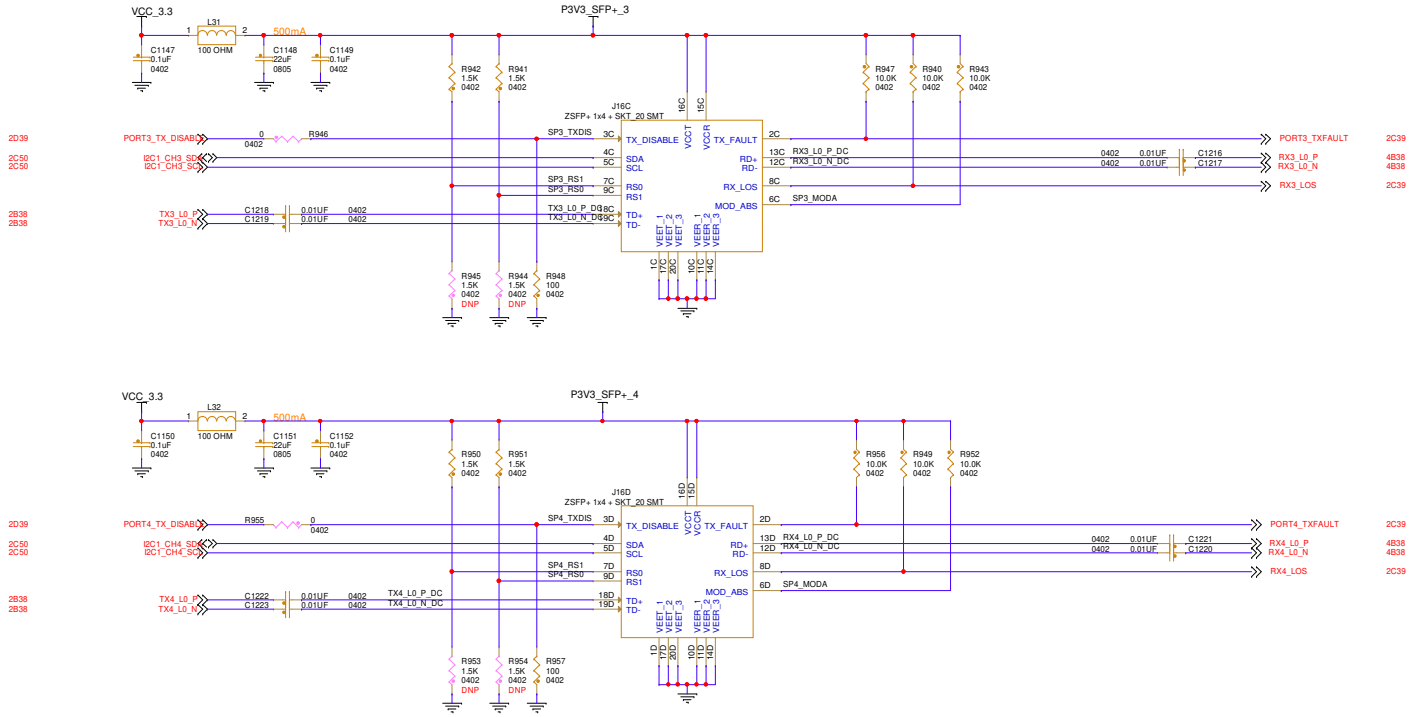
SFP Ports 3 & 4



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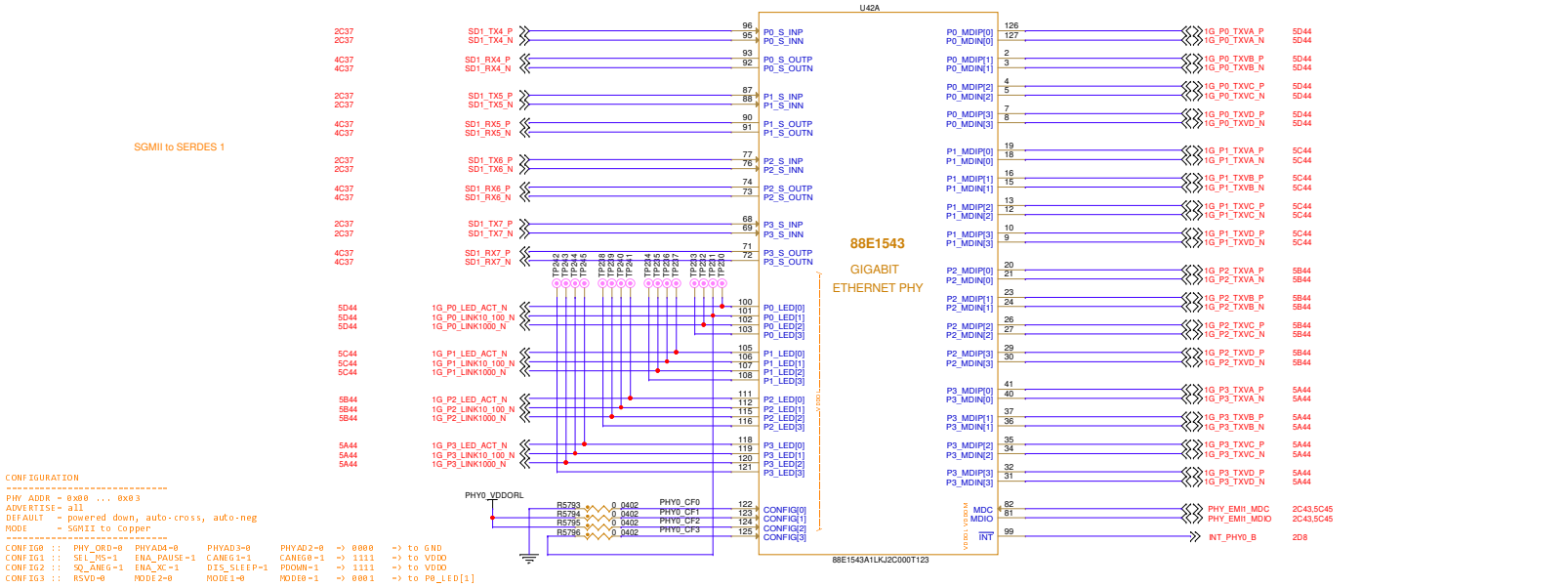
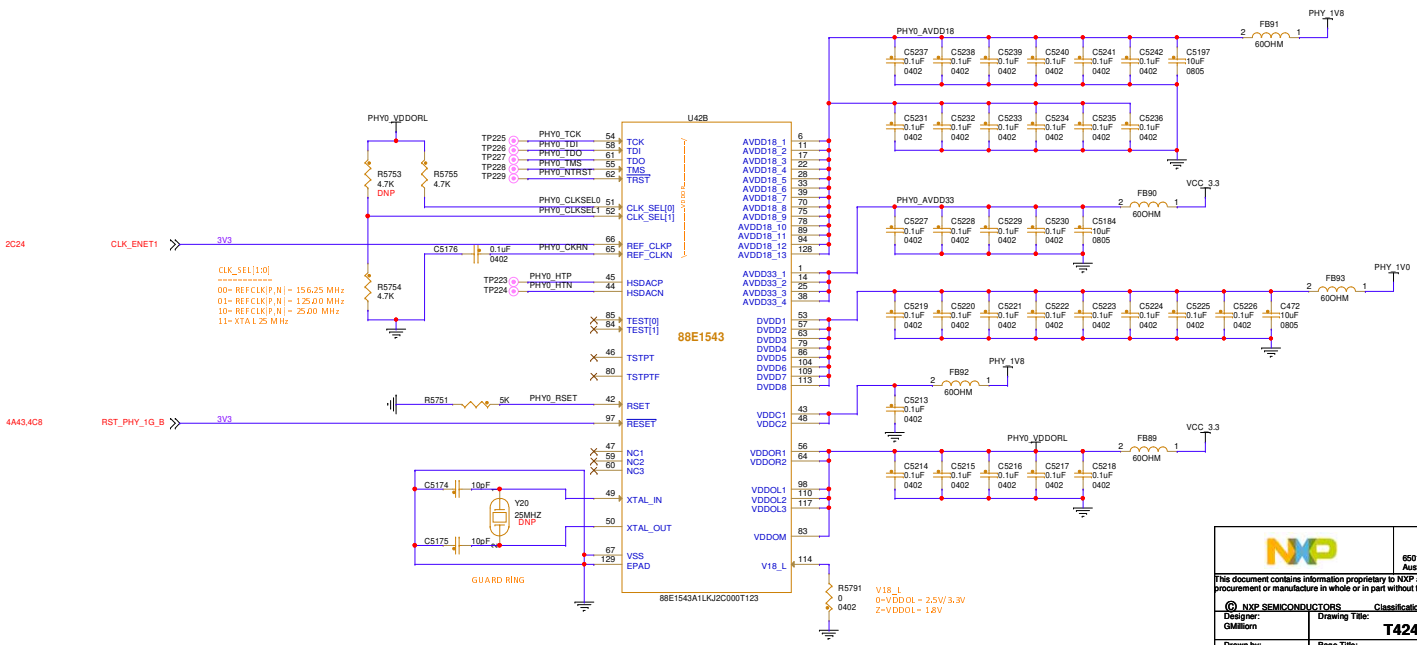
1GE PHY #1





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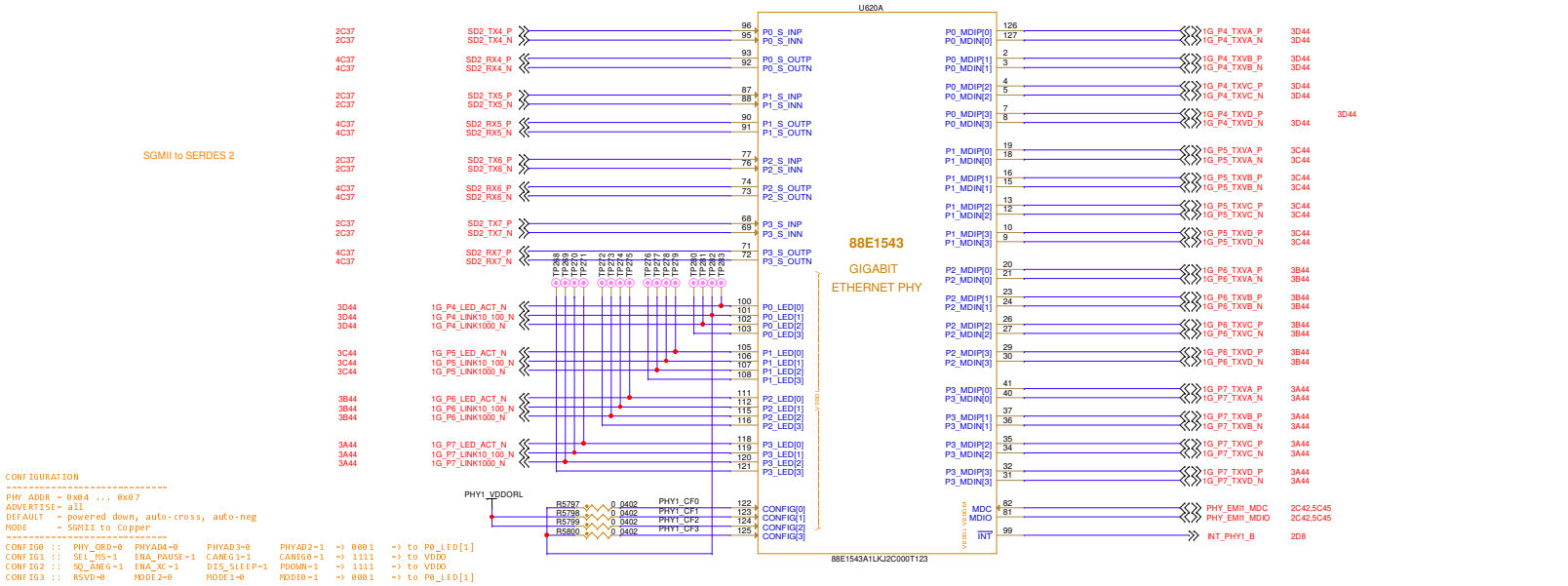
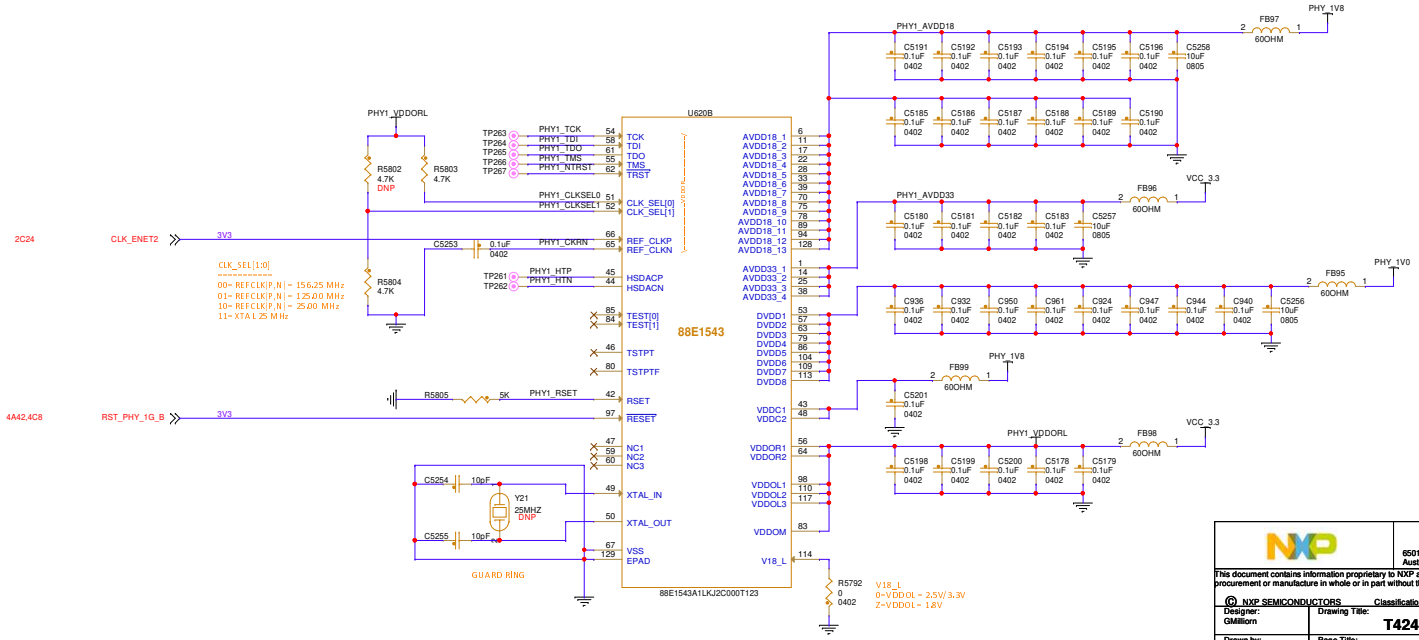
1GE PHY #2





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1GE PORTS 1-8

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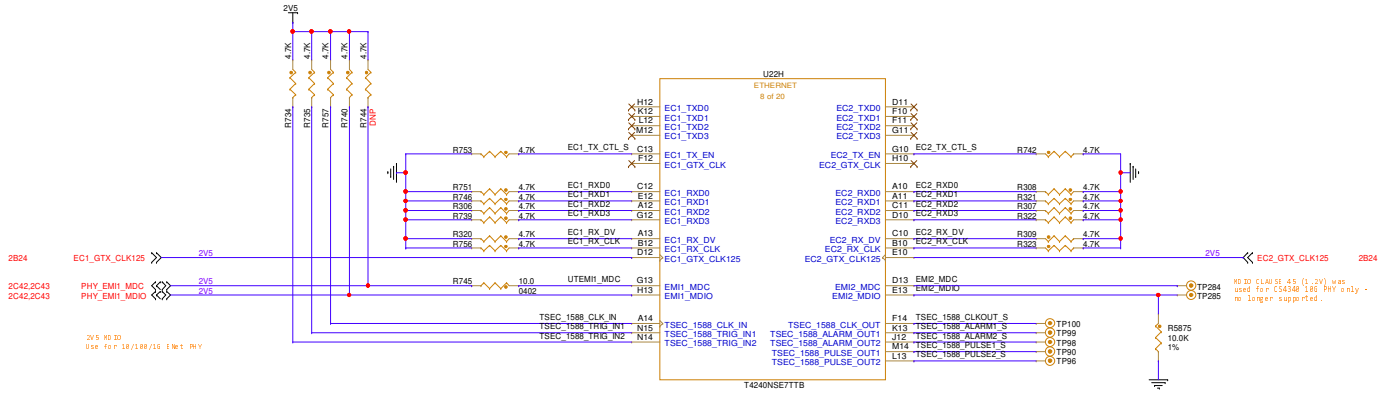
T4240 MDIO + RGMII



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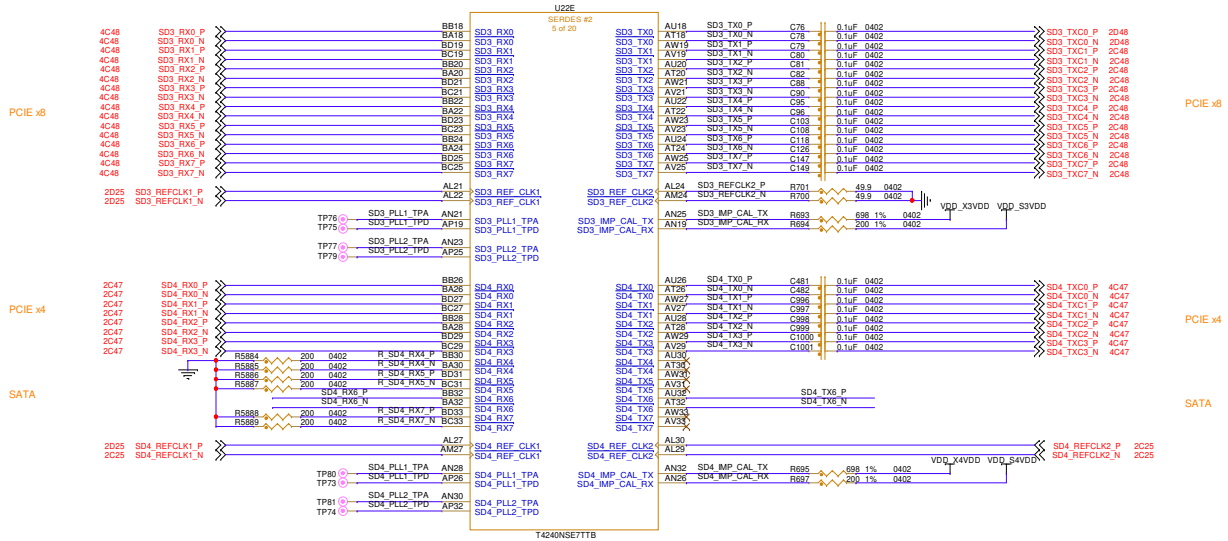
BACK SIDE SERDES 3 & 4 (PCIe / SATA)



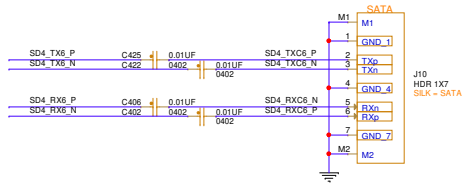


Table 18-5. SerDes 3 Options

SRDS_PRTCL_S3		SerDes 3								
Decimal	Hex	A	B	C	D	E	F	G	H	Per Lane PLL mapping
1	1	PCIe1 (5/2.5)								11111111
2[1]	2	PCIe1 (5/2.5)				PCIe2 (5/2.5)				11111111

```
SerDes 3 configuration
==================================================
RCW[SRDS_PRTCL_S3]=            1- PCIe1 x8
PLL mapping=                   11111111
RCW[SRDS_PLL_PD_S3]=           01
RCW[SRDS_PLL_REF_CLK_SEL_S3]= 0: PLL1=100MHz
```

Table 18-6. SerDes 4

SRDS_PRTCL_S4		SerDes 4								
Decimal	Hex	A	B	C	D	E	F	G	H	Per lane PLL mapping
1	1	PCIe3 (5/2.5)								11111111
3[1]	3	PCIe3 (5/2.5)				PCIe4 (8/5/2.5)				11111111
5	5	PCIe3 (5/2.5)				SRIO2 (5/2.5)				11111111
7	7	PCIe3 (8/5/2.5)				SRIO2 (3.125)				11112222
9	9	PCIe3 (5/2.5)				PCIe4 (5/2.5)		SATA1 (3/1.5)	SATA2 (3/1.5)	11111122

```
SerDes 4 configuration
==================================================
RCW[SRDS_PRTCL_S4]=            9/11- PCIe3 x4, Unused x2, SATA1 & Unused
PLL mapping=                   11111122
RCW[SRDS_PLL_PD_S4]=           00
RCW[SRDS_PLL_REF_CLK_SEL_S4]= 00: PLL1=100MHz & PLL2=100MHz
```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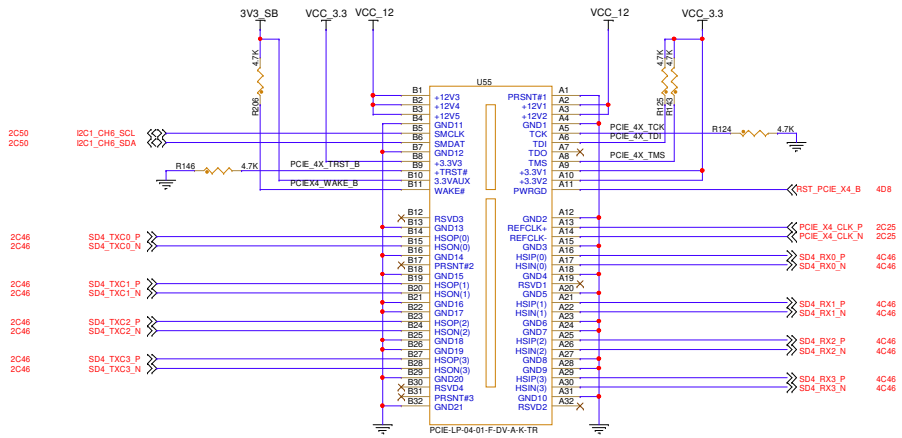
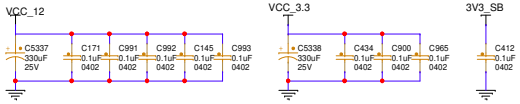
PCIE SLOT #1: x4





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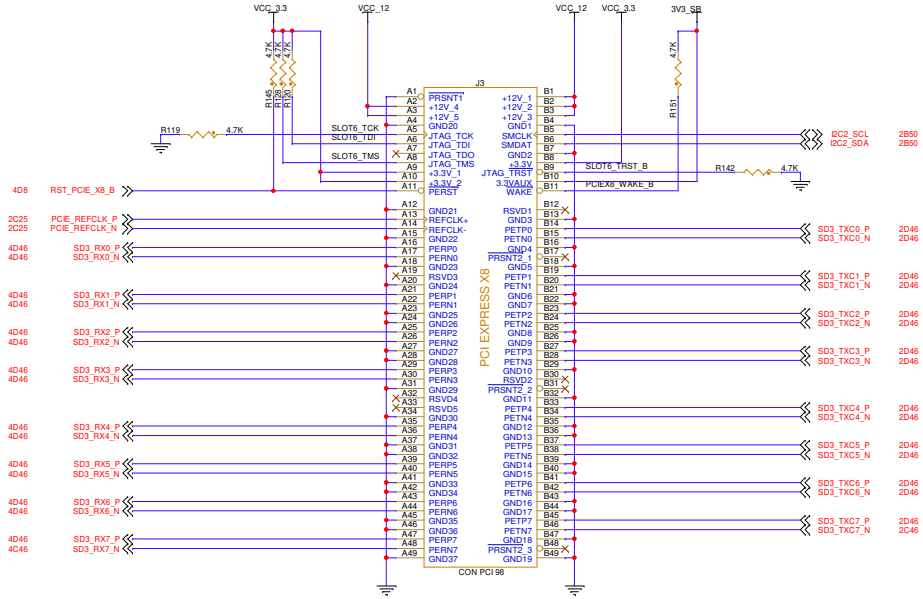
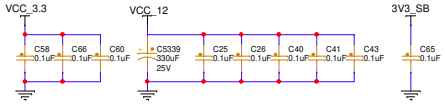
PCIE SLOT #2: x8





VCC_12 : 2100mA
VCC_3.3 :3000mA

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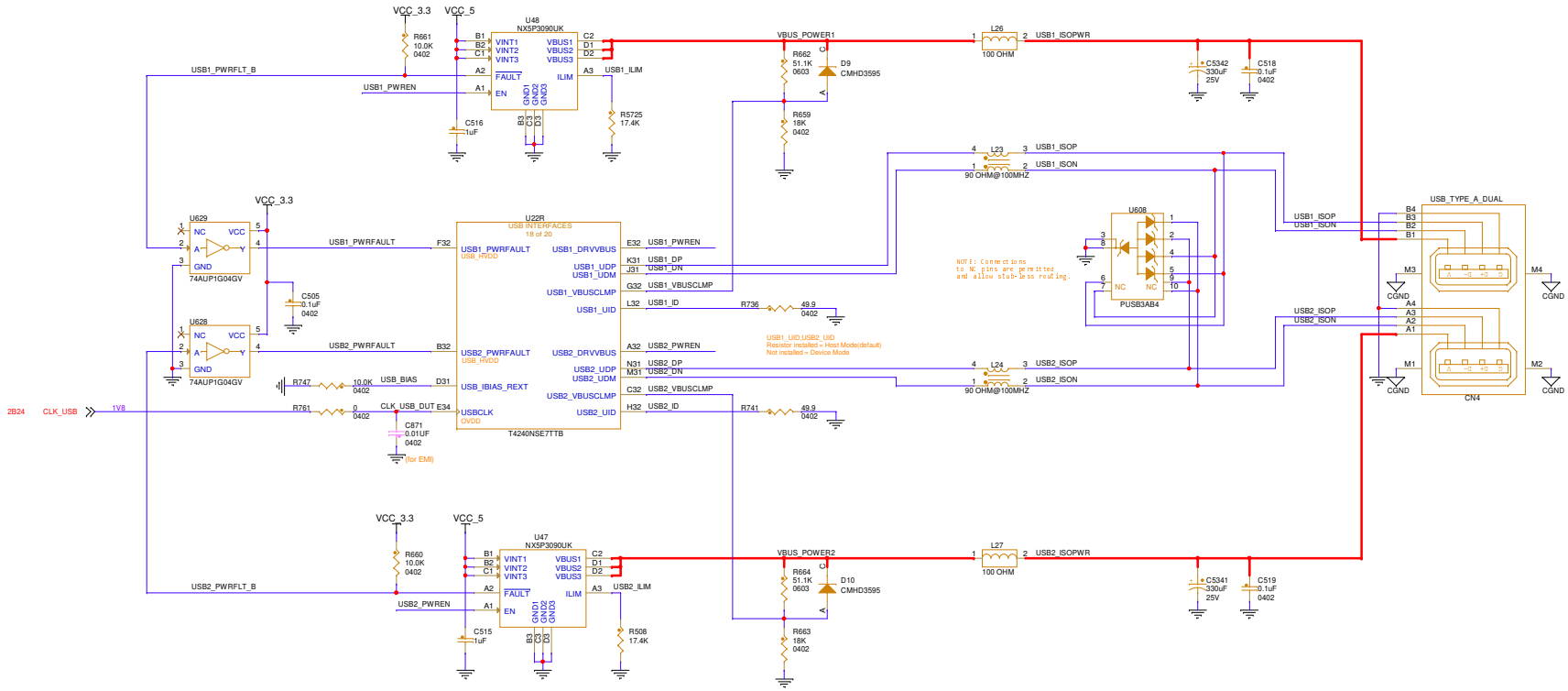
USB PORTS



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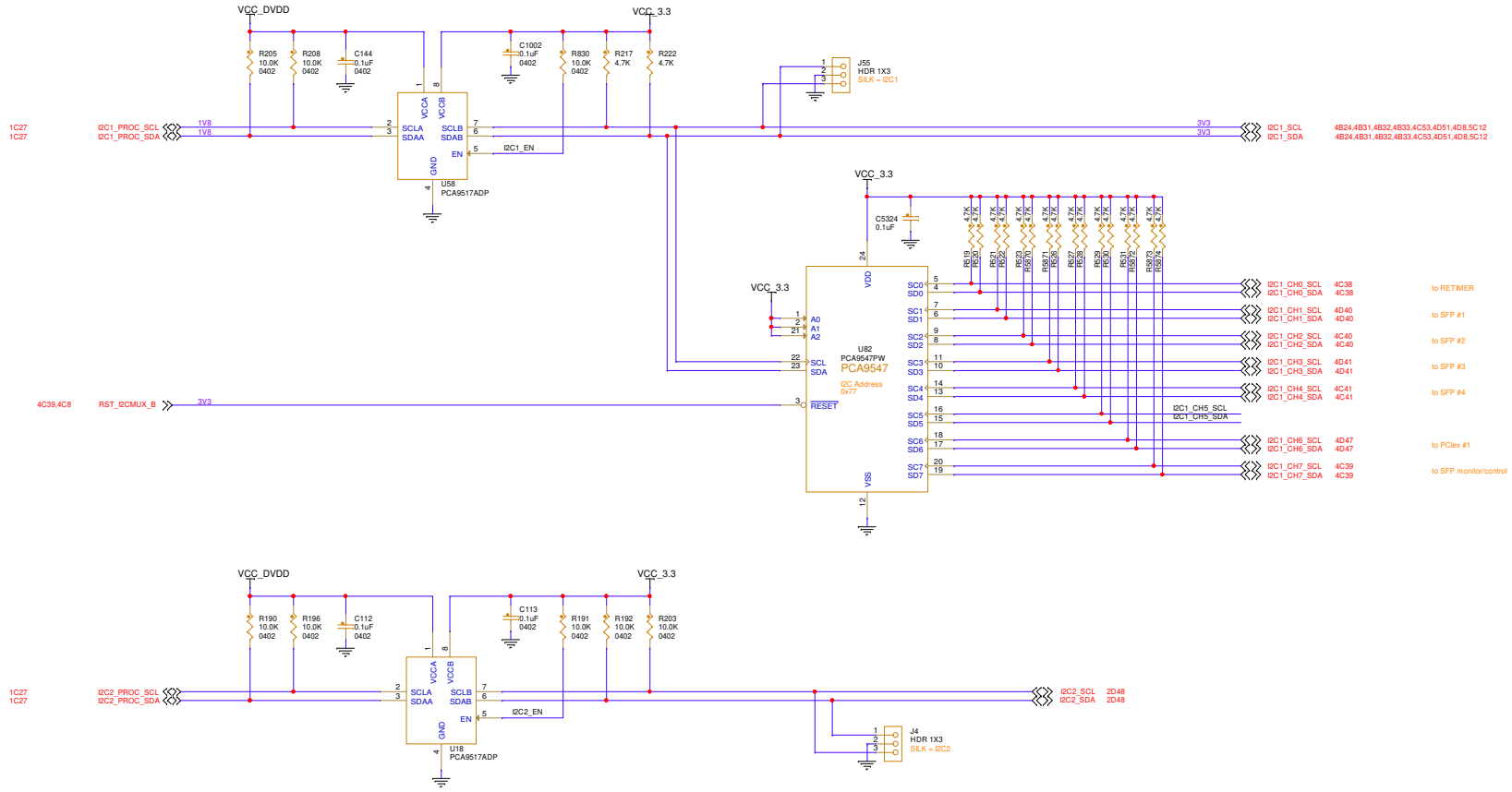
I2C BUS TRANSLATION & MUX



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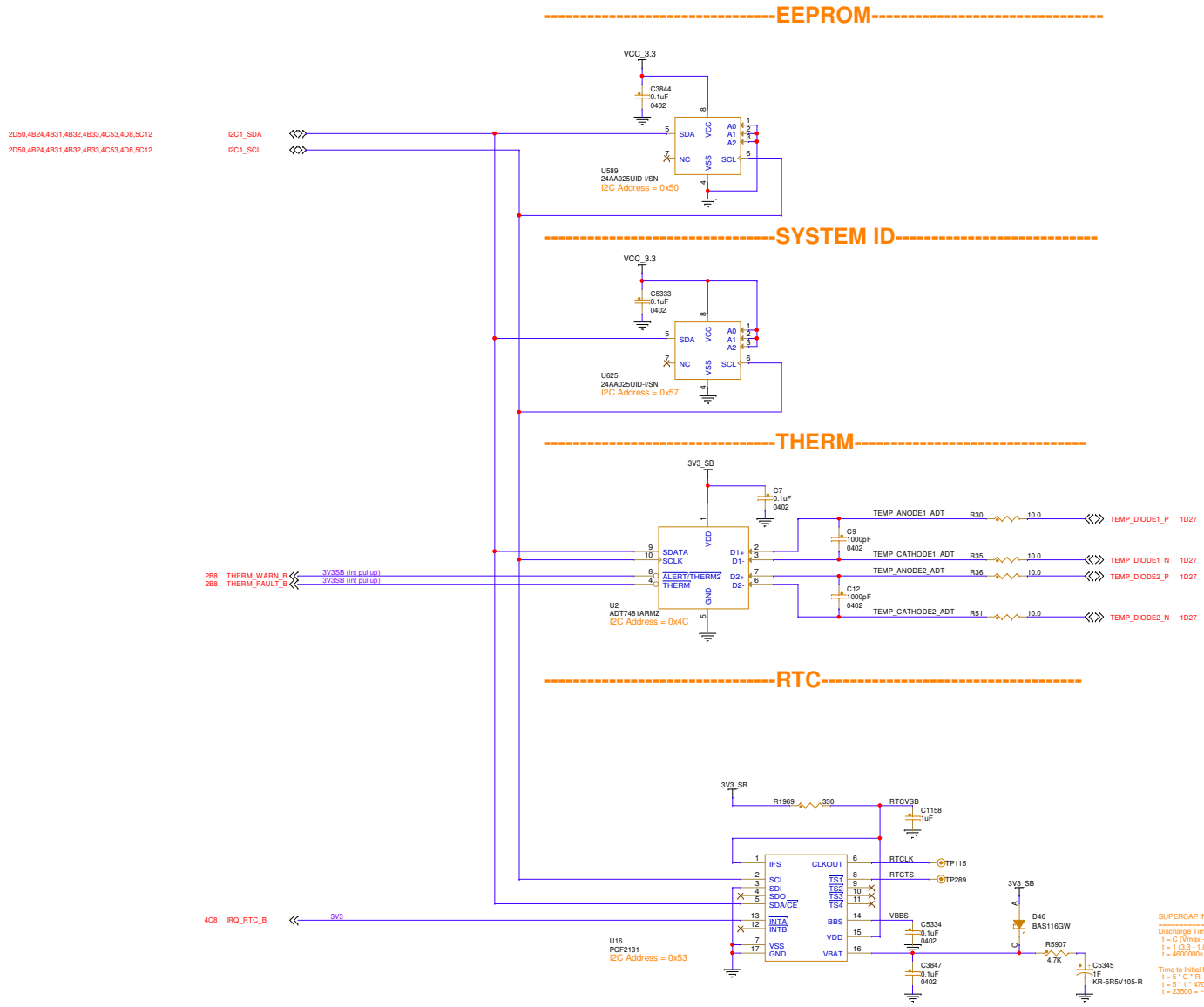
Drawn by: GMillorn	Page Title: I2C Bus Translation & Mux		
Approved: DN_Apps	Size C	Document Number SCH-27749 / PDF: SPF-27749	Rev E
	Date: Tuesday, November 21, 2023	Sheet 50 of 55	

I2C BUS DEVICES



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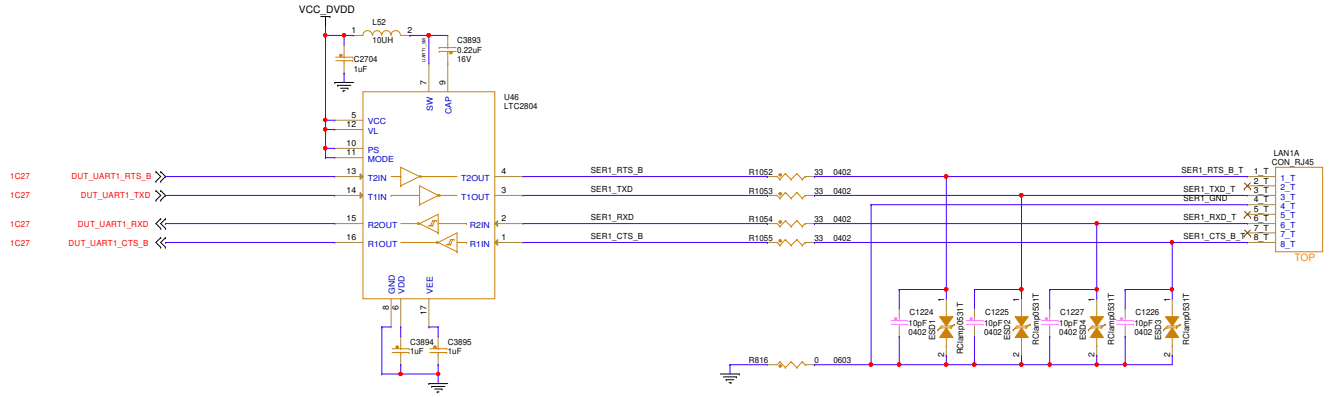
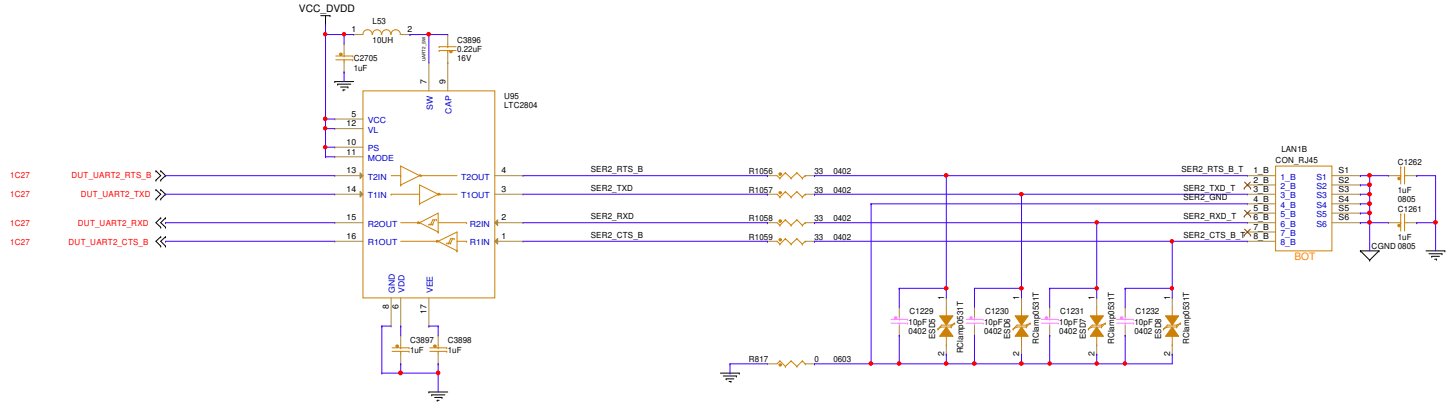
UART PORTS





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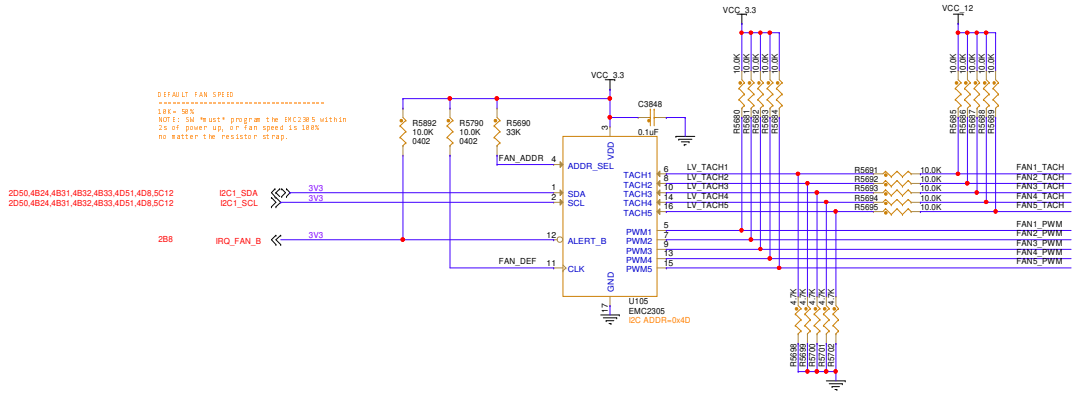
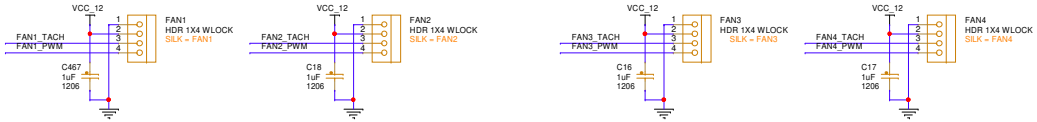
FAN CONTROLLER & HEADERS





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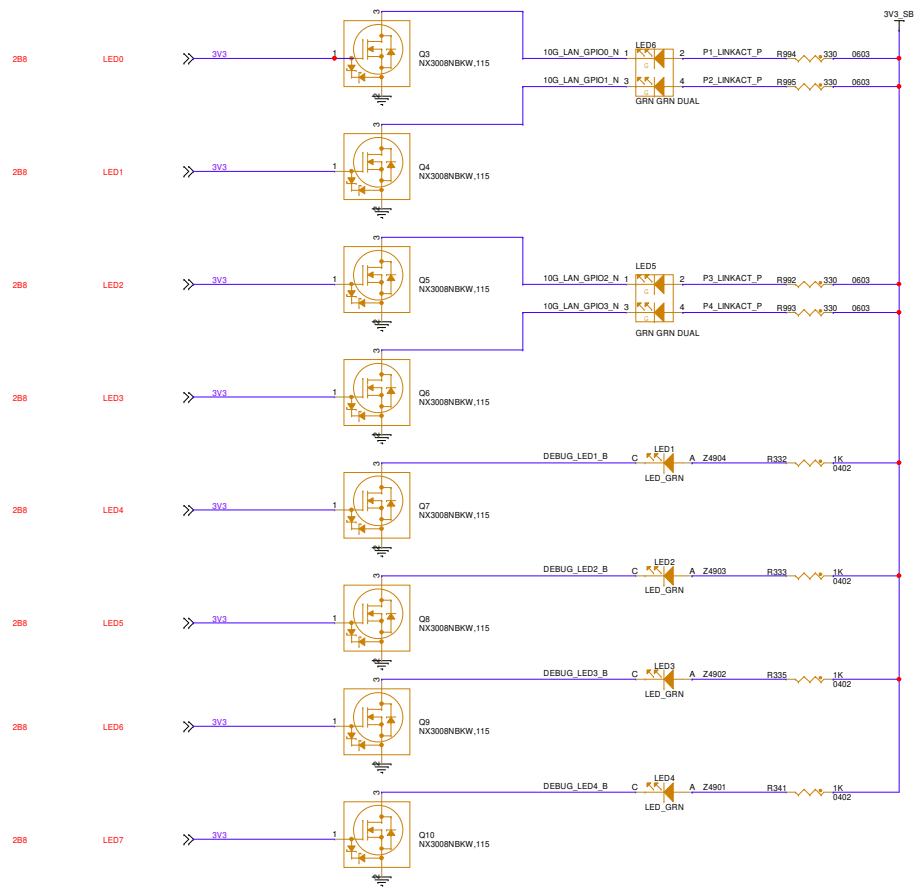
LEDs



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ASSEMBLY INFO

REF DES	JUMPER	PAGE NAME
JP6	1-2	051- I2C Devices

REF DES	ASSY_OPT	PAGE NAME
R748	DNP	006- Power Entry & Mechanical
JP8	DNP	008- System FPGA IO Ports
J69,JP7,U250	DNP	009- System FPGA Power+Prog
R5771	DNP	010- Switches and Config
C5132,R95	DNP	011- GVDD & OVDD Power
R42,R628,R629	DNP	012- VDD
CT24,CT29,CT41,R273	DNP	020- T4240 GVDD+Other Power
R5762	DNP	027- T4240 System Block + COP
C485	DNP	036- T4240 SPI / SDHC Port
R532,R533,R534,R535,R536, R537,R538,R539,R730,R731	DNP	037- T4240 SerDes 1 & 2
R5825,R5826,R5827,R5828, R5837,R5838,R5839,R5840	DNP	038- 10G Retimer
R926,R927,R935,R936	DNP	040- SFP Ports 1&2 + Cage
R944,R945,R953,R954	DNP	041- SFP Ports 3&4
R5753,Y20	DNP	042- 88E1543 1G Phy #1
R5802,Y21	DNP	043- 88E1543 1G Phy #2
R744	DNP	045- T4240 EMI + RGMII
C871	DNP	049- T4240 USB Ports
C1224,C1225,C1226,C1227, C1229,C1230,C1231,C1232	DNP	052- Serial Ports

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